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# MS-7996

ATX:235\*180

Ver: 13

## Intel -SkyLake-S plamform

### CPU:

LGA1151  
CPU POWER PAK \*3 Phase  
GT POWER PAK \*2 Phase

### System Chipset:

SPT-H :B150  
SPT-H :H150

### Onboard Chip:

HD Audio Codec: ALC892  
SIO: NCT5563D  
Flash ROM: SPI 64 MB  
DP to VGA: ITE6515

### PWM:

VCORE - RT3606  
DDR - RT8231  
PCH(1.0V) - UP1540  
VCCSA - RT8125C  
VCCIO - NB681(Converter)  
VPP25 - MP2147

### Main Memory:

DDR4 \* 2 (Dual Channel)

### LDO:

VCCSTPLL - GS7133

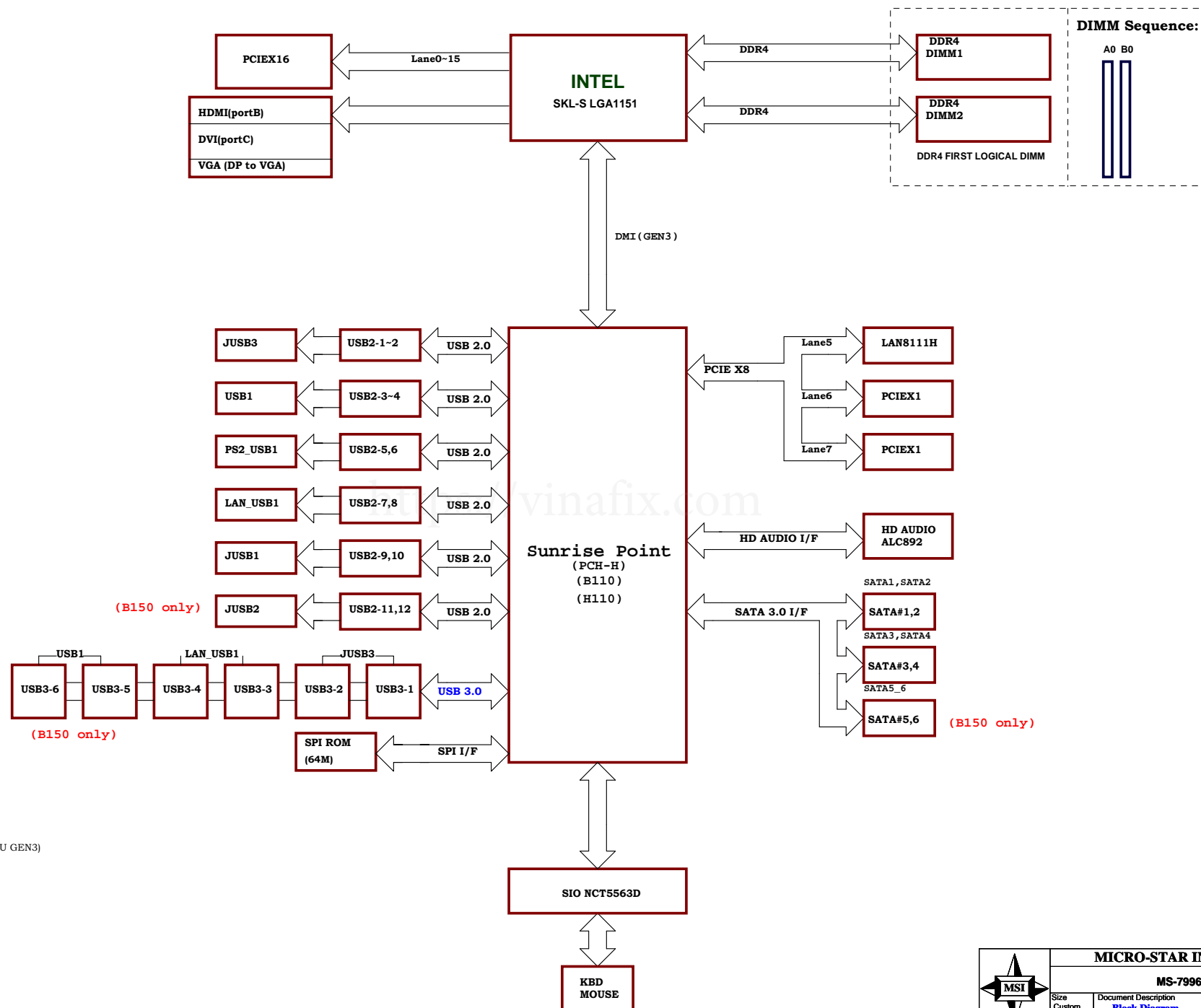
### ACPI:

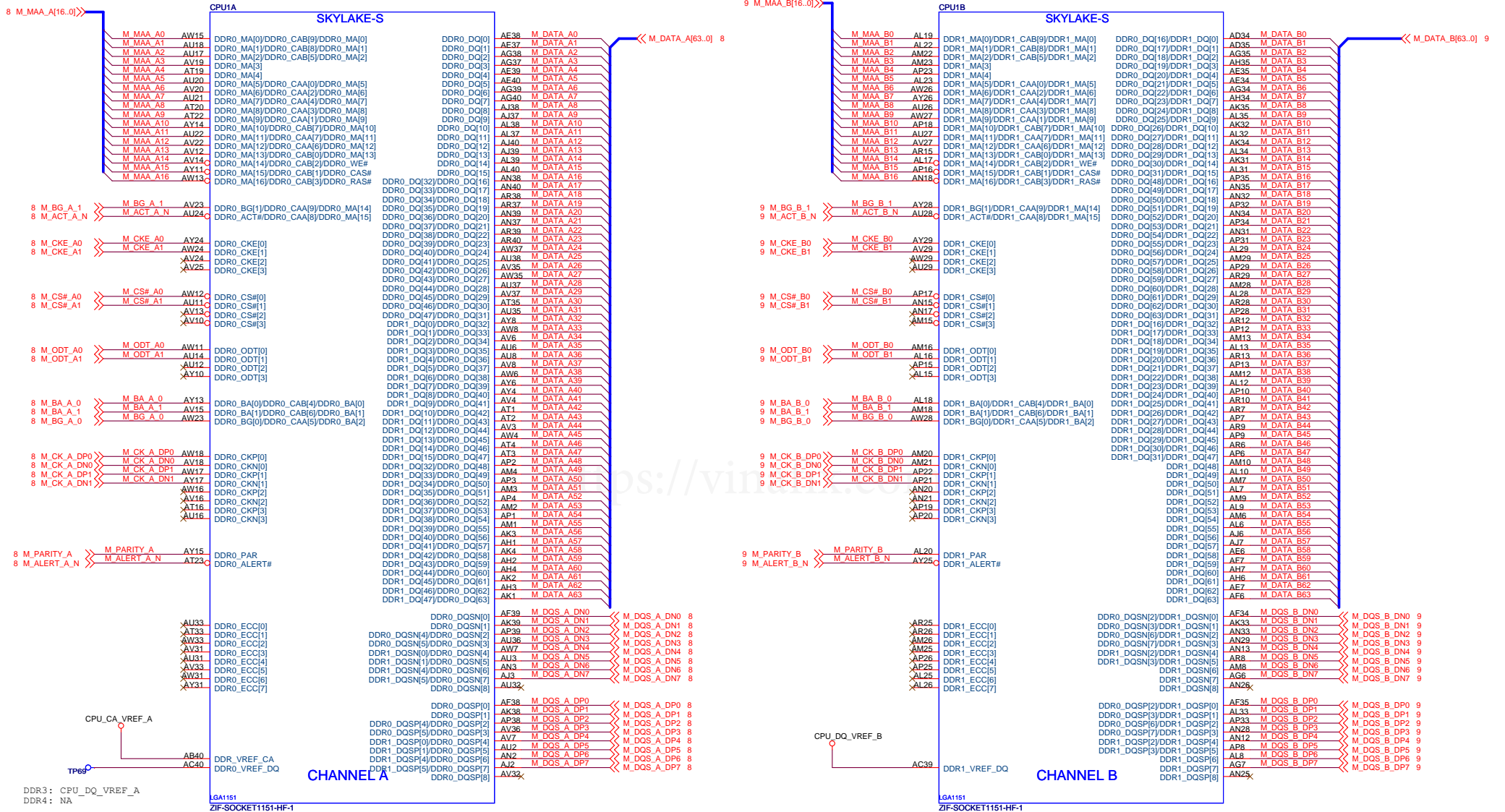
5VDAUL:uP7501  
5VDIMM:uP7501  
3VSB:GS7133+PN MOS  
3VDSW:GS7133

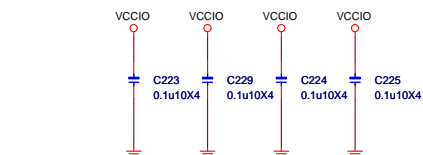
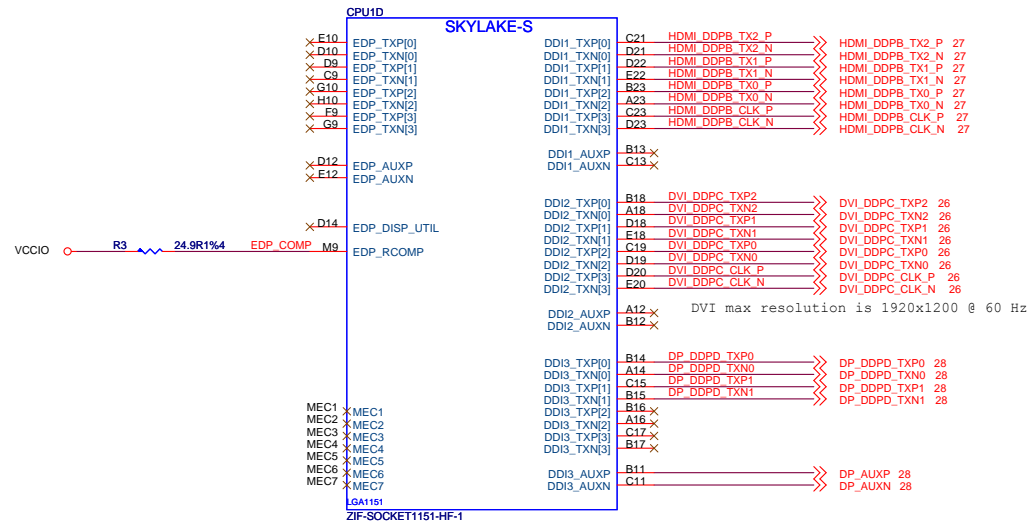
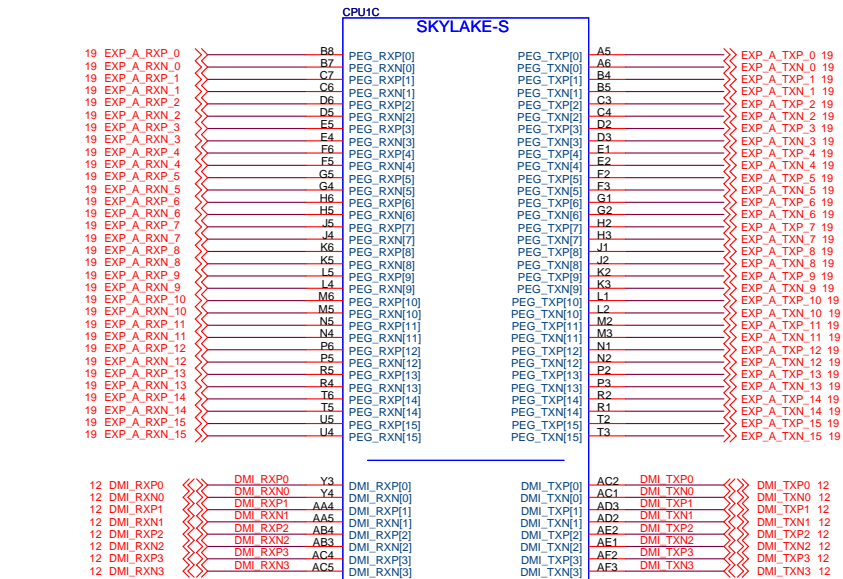
### Expansion Slots:

PCI Express (X16) Slot \* 1  
PCI Express (X1 ) Slot \* 2

## MS-7996 Block Diagram



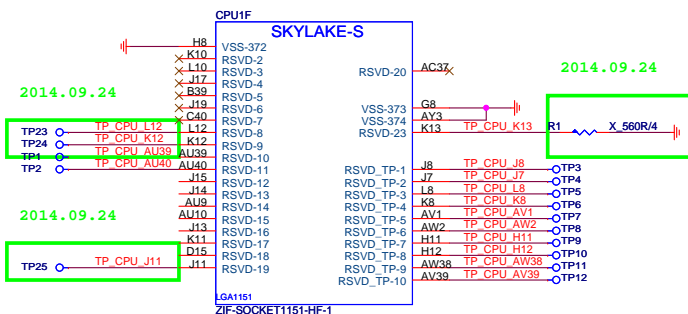




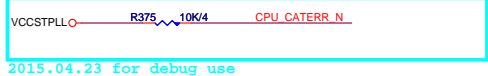
For DMI reference VCCIO USE  
please close to DMI via side

CRB 1.0 update  
Add TP23,TP24  
For Test

CRB 1.0 update  
TP25  
For Test

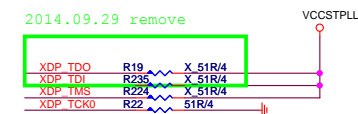
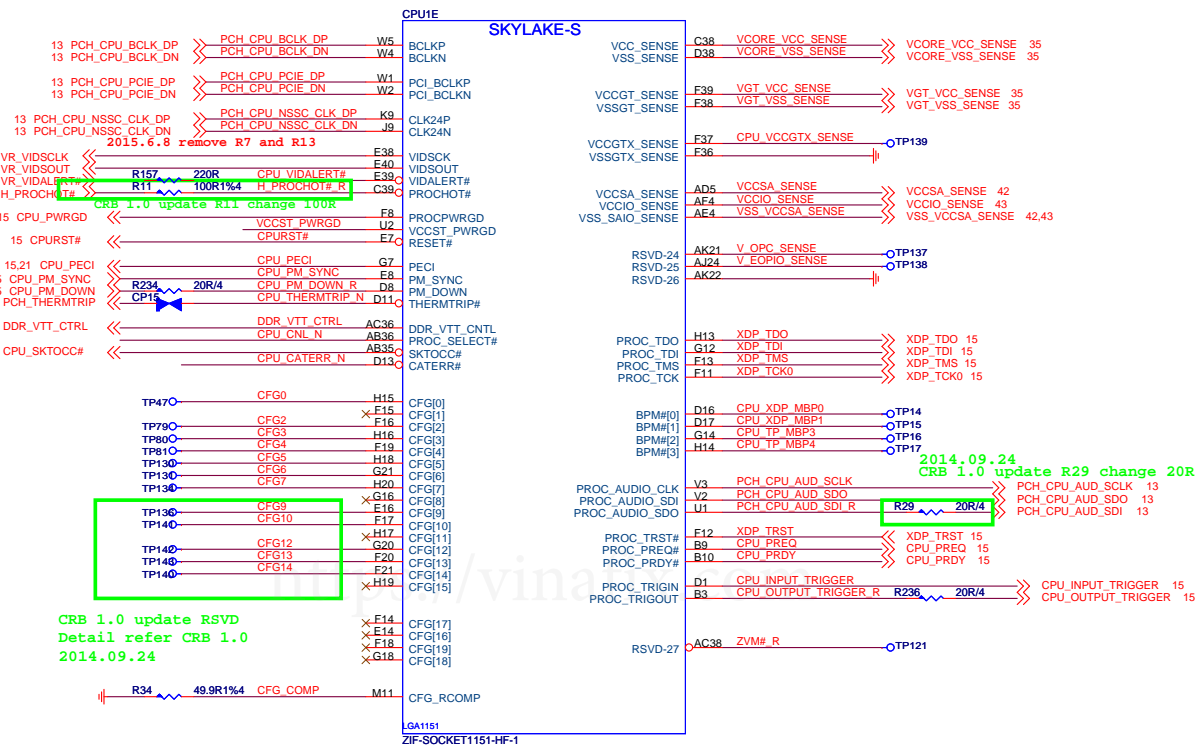


2014.09.24  
CRB 1.0 update  
CRB unstuff  
PCB come back remove



CFG Strap

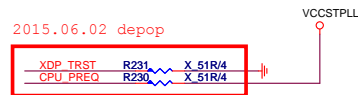
CFG Table			
	HIGH	LOW	SEL LOCK
0	No Lock	LOCK	PCU RSDVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSDVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG OVFLOW TRAINING
8			RSDVD
9			RSDVD
10			RSDVD
11			RSDVD
12			RSDVD
13			RSDVD
14	RSDVD		
15	RSDVD		



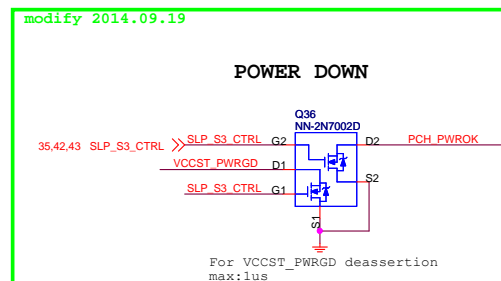
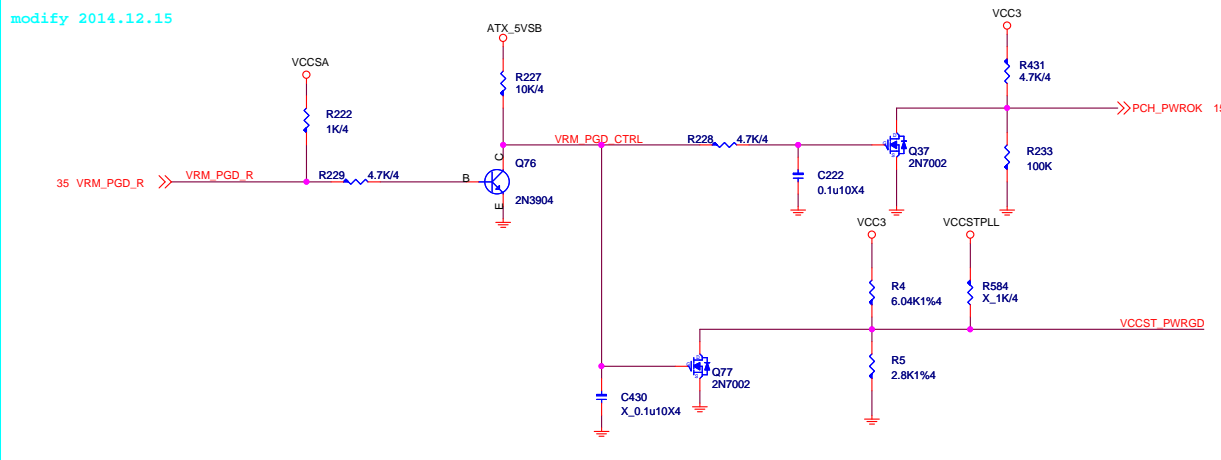
```

    Close CPU <1100 mil
    1000 mil < CPU XDP MBP0~1 < 6000 mil

```



2015.06.02 depop



```
For VCCST_PWRGD deassertion
max:lus
```

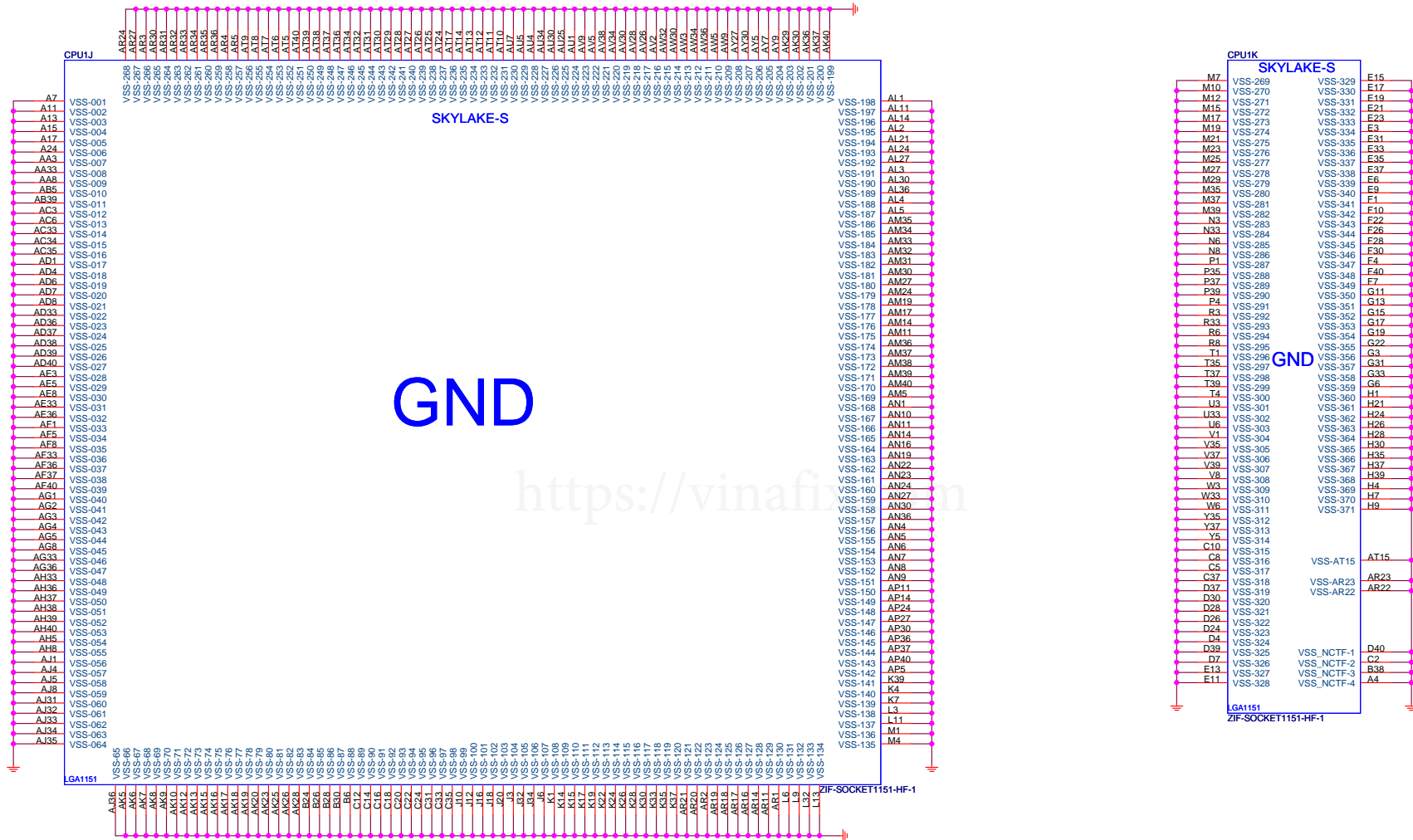


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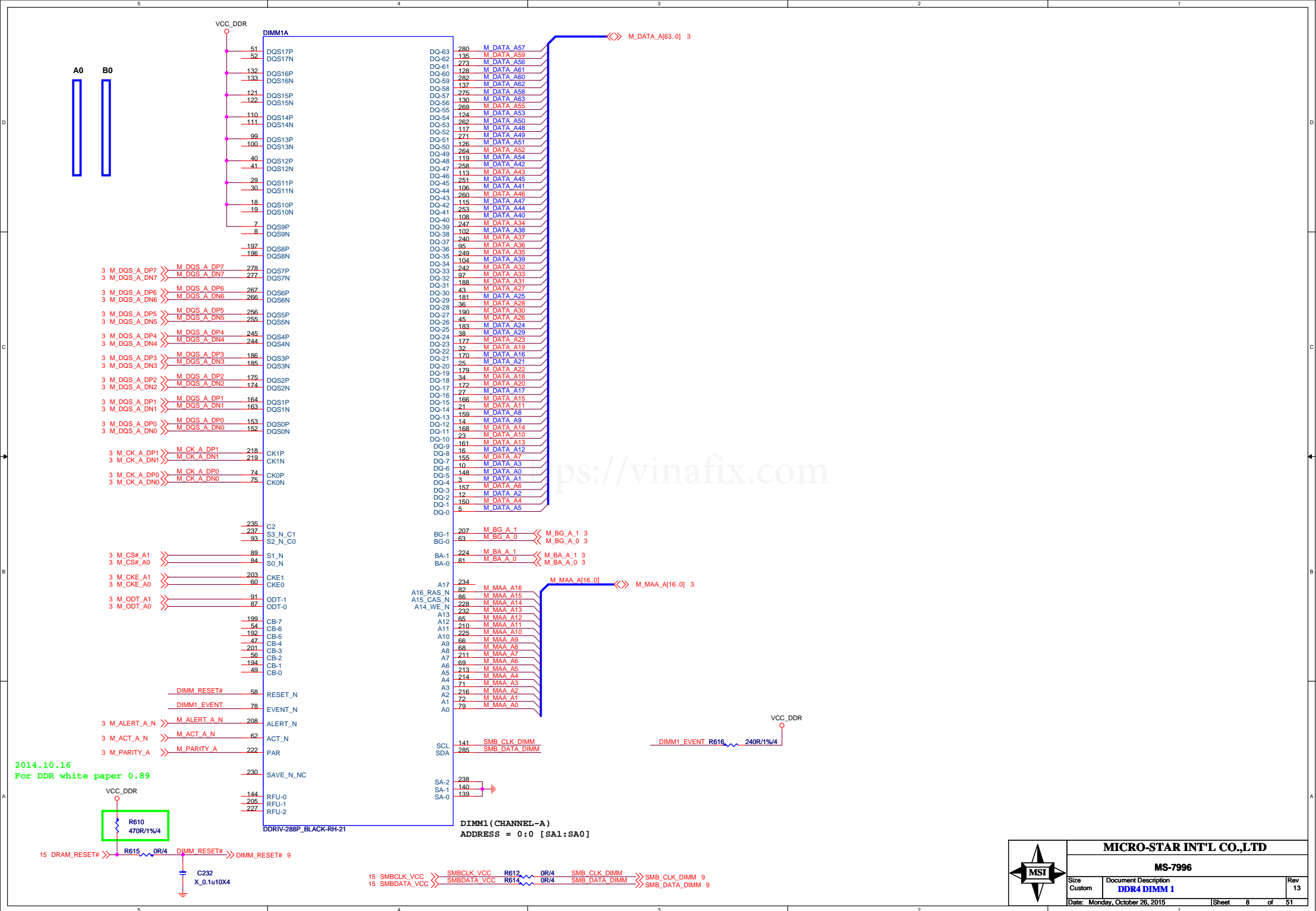
**MS-7996**

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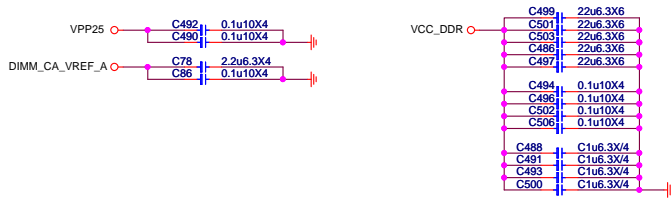
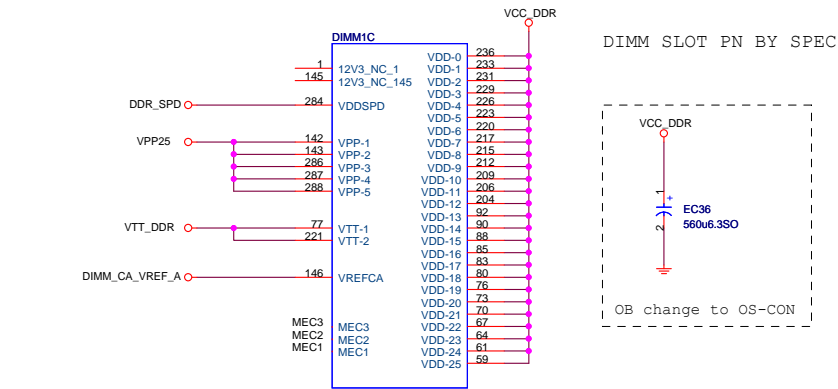




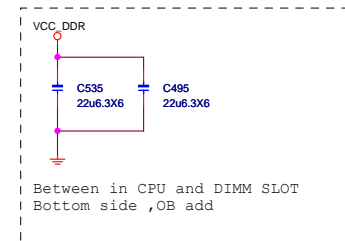
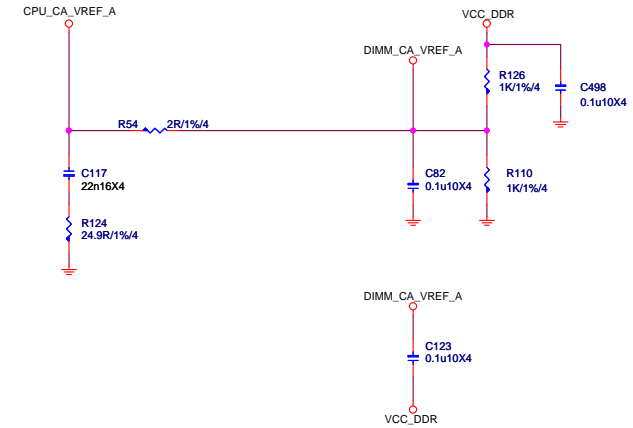
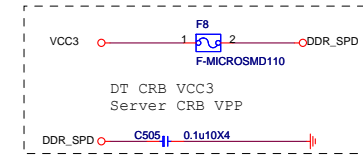
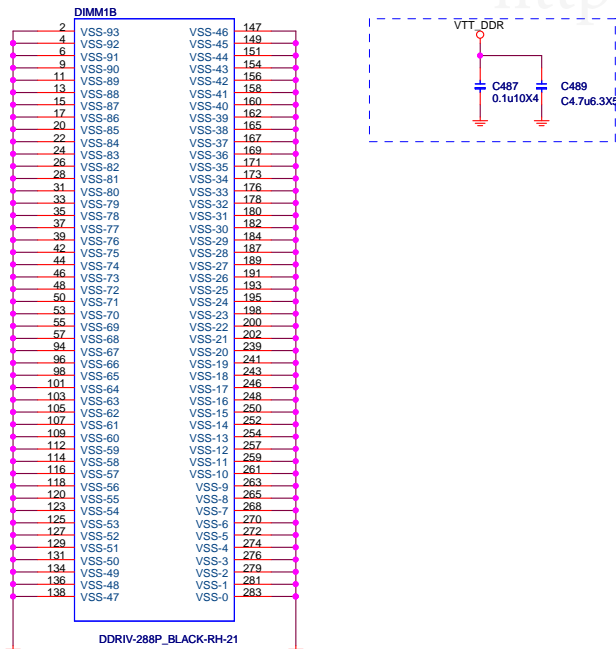


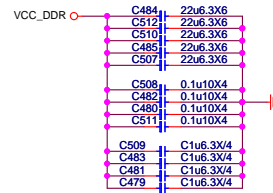
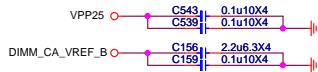
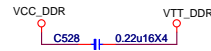
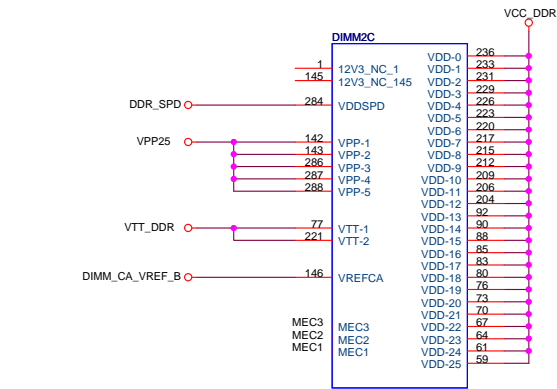






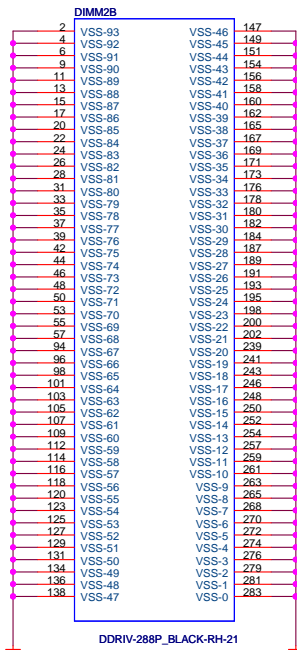
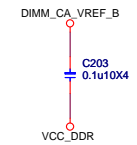
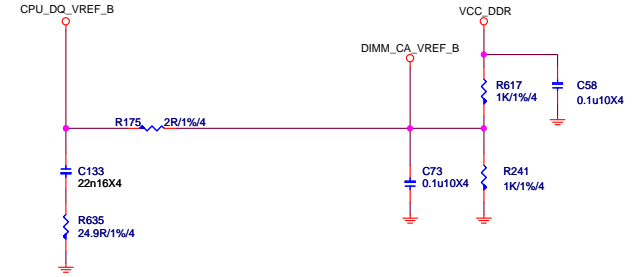
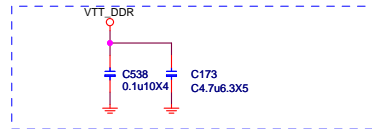
0.1uFxl per dimm

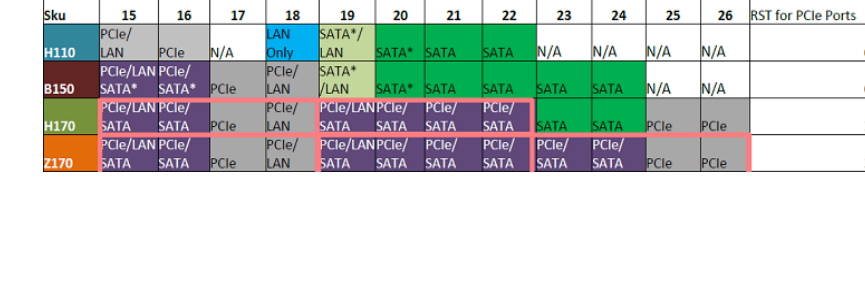
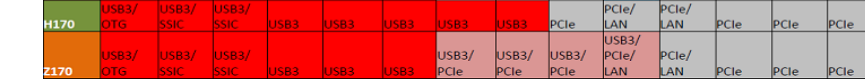
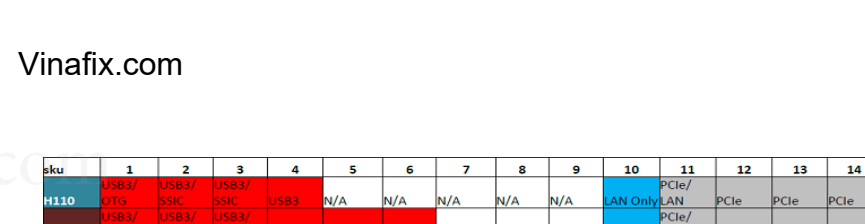
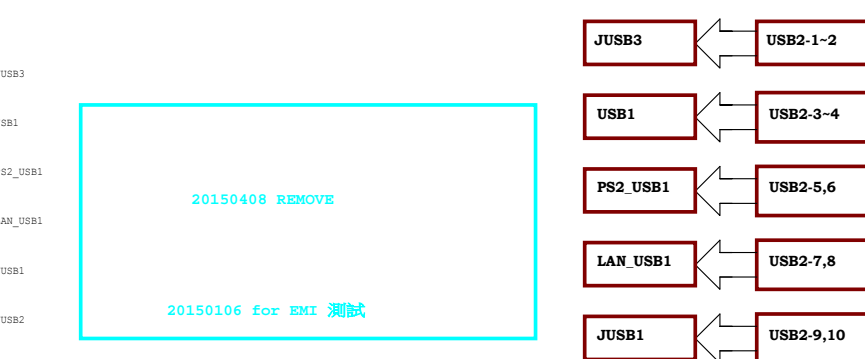
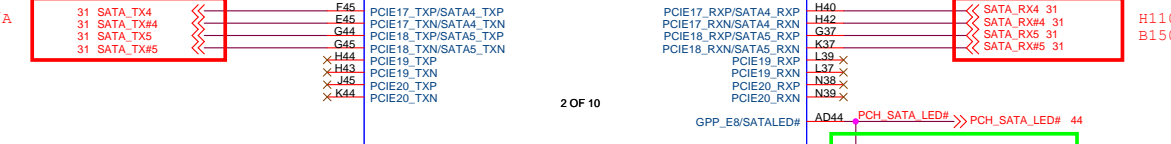
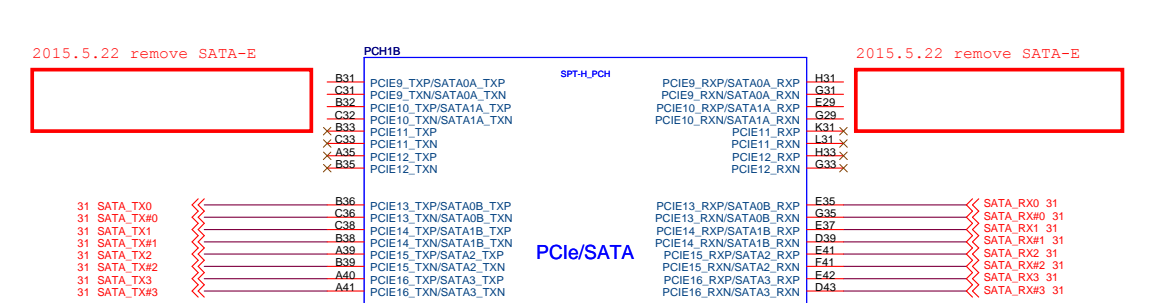
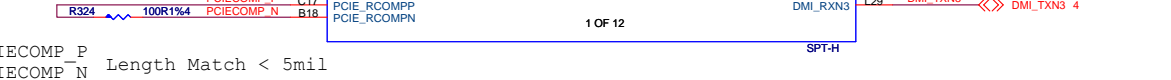
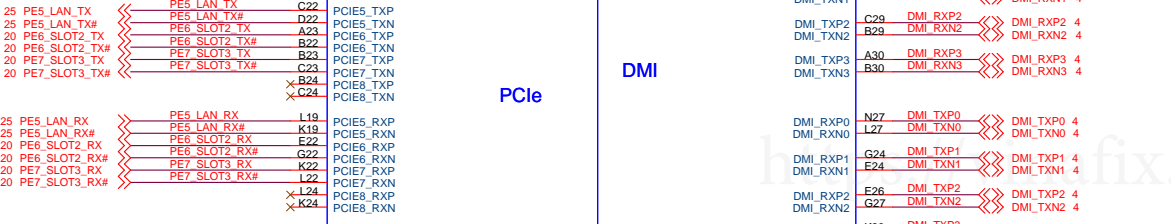
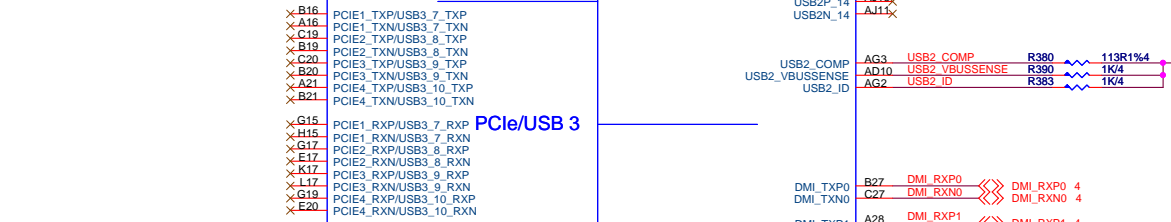
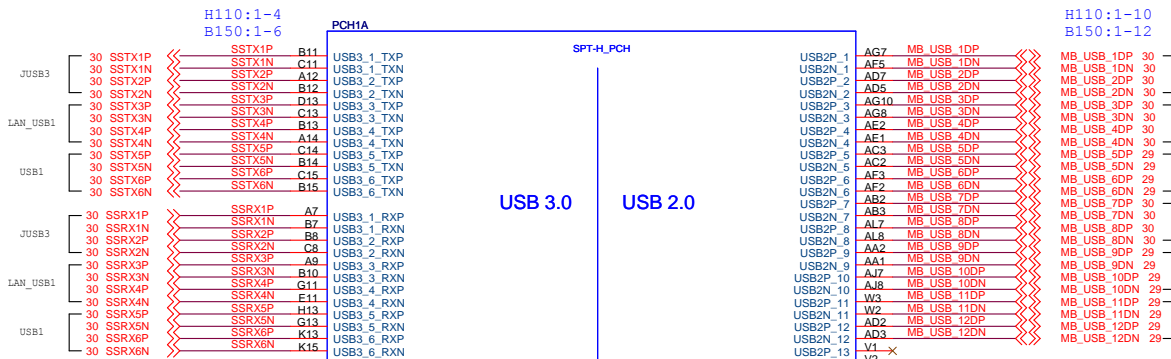




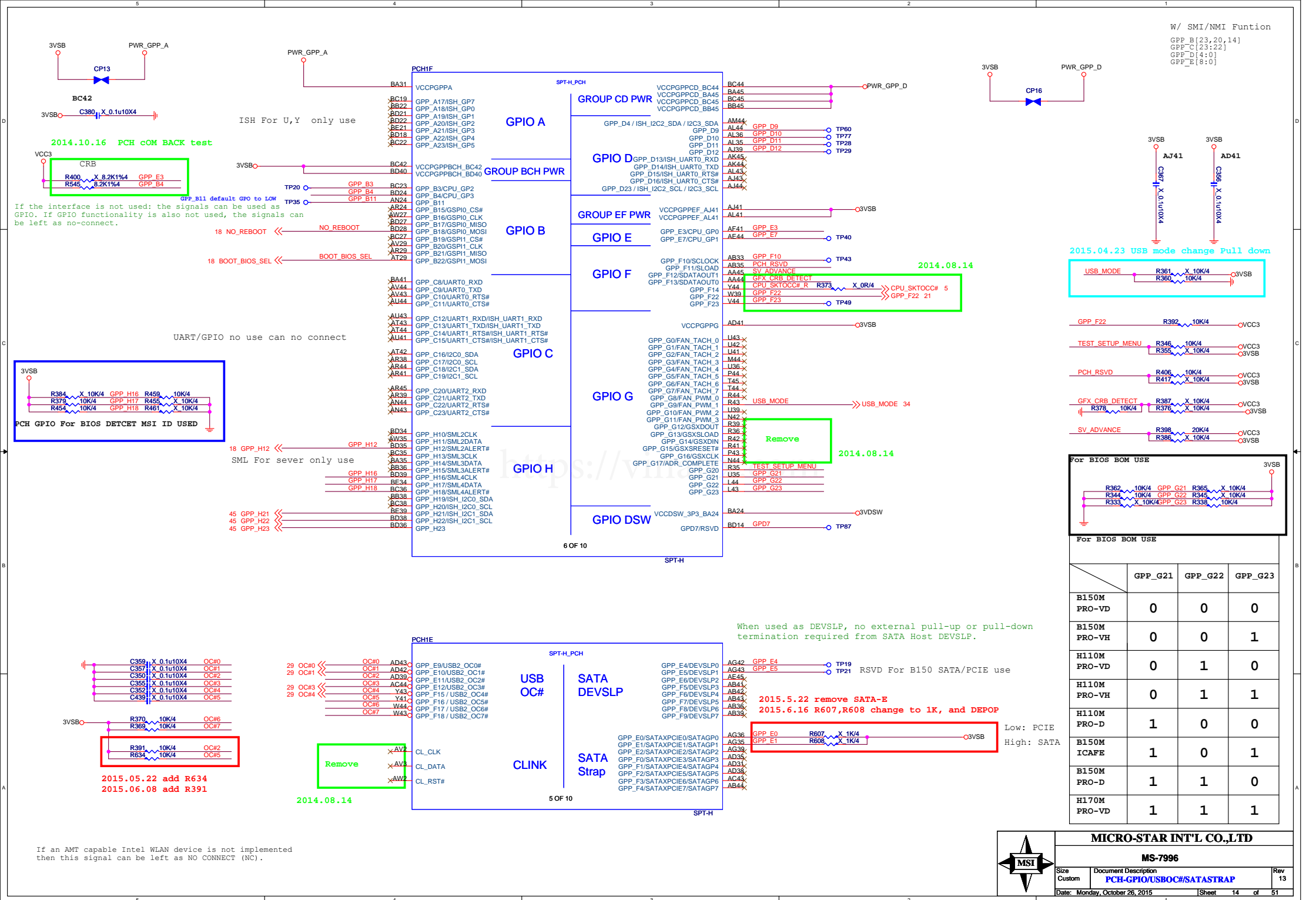
<https://vinafix.com>

0.1uFxl per dimm















GND

<https://vinafix.com>

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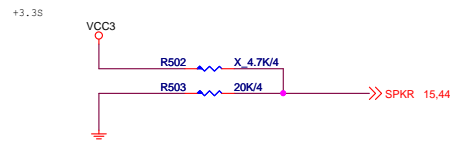


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## TOP Swap



Internal pull-down 20K is disabled after PLTRST#

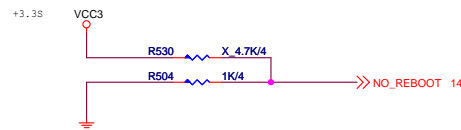
## LPC eSPI Mode



0 : LPC  
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

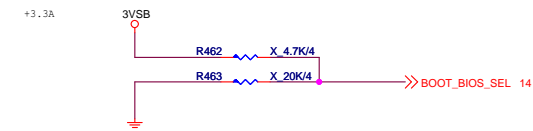
## No Reboot



0 : DISABLE (Default)  
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

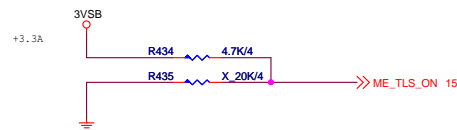
## Boot BIOS



0 : SPI  
1 : LPC

Internal pull-down 20K is disabled after PLTRST

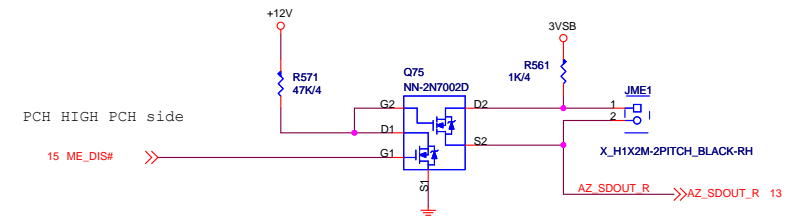
## AMT and SBA with confidentiality



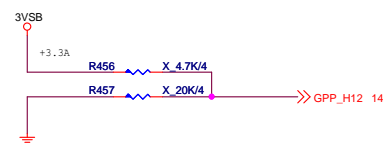
0 : DISABLE  
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

## HDA\_SDO



## ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING  
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST



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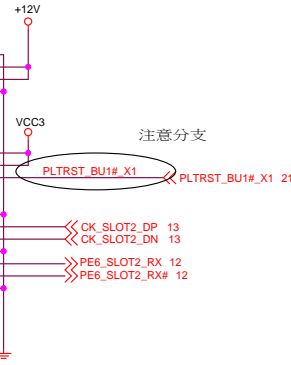
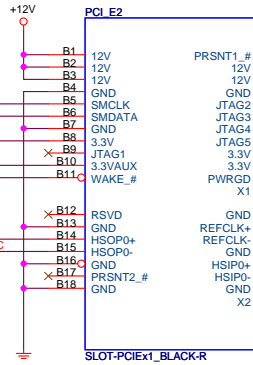
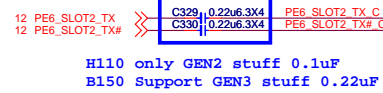
MS-7996

Size Custom	Document Description <b>PCIE SLOT-CPU(X16)</b>	Rev 13
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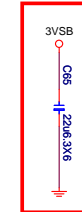
2015.6.8 change net\_name to SMBCLK\_VSB and SMBDATA\_VSB



2014.12.29



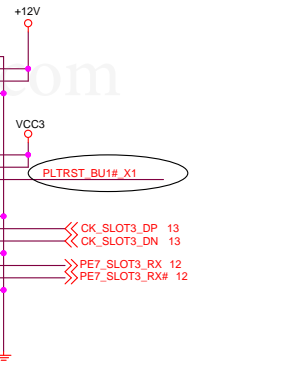
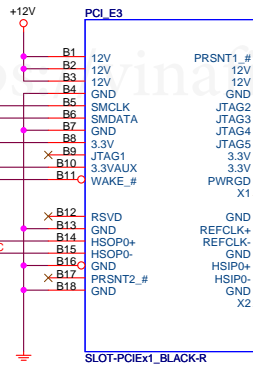
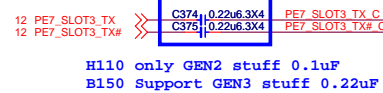
2015.6.16 add C65



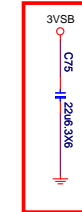
2015.6.8 change net\_name to SMBCLK\_VSB and SMBDATA\_VSB



2014.12.29



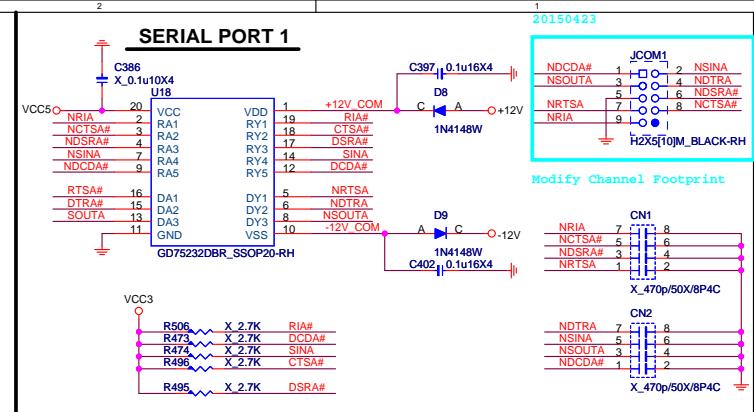
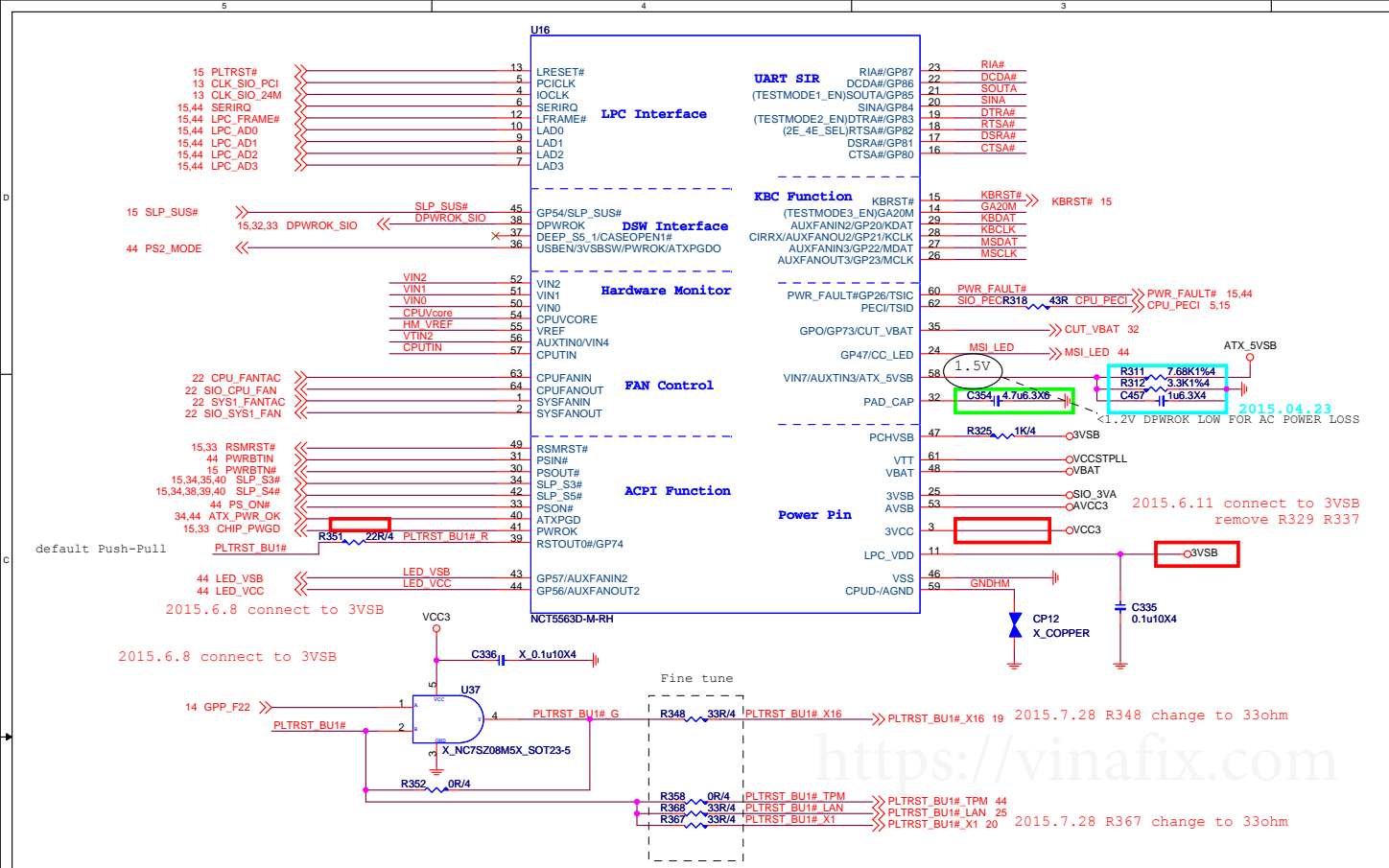
2015.6.16 add C75



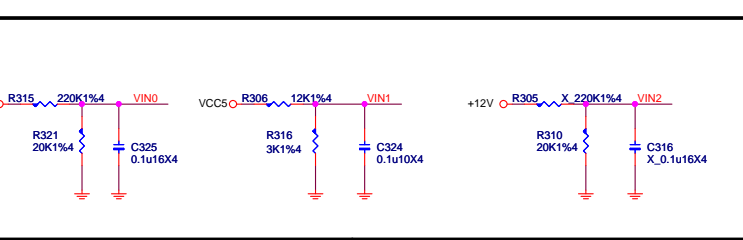
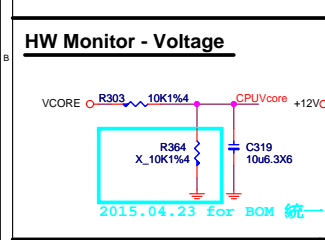
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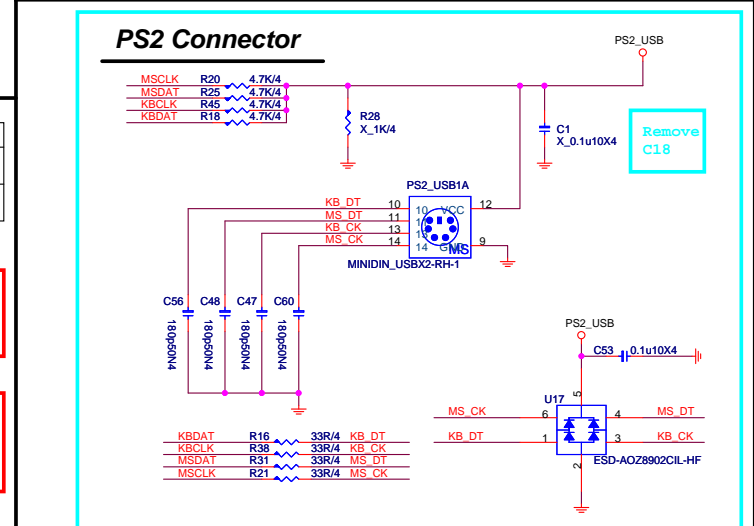
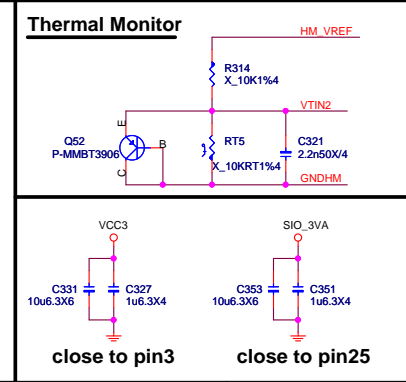
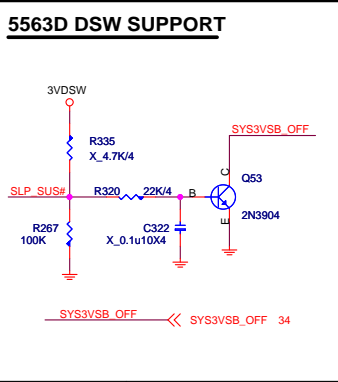
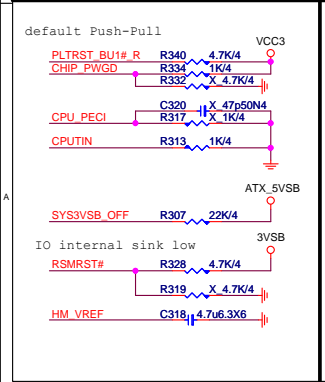
POWER ON STRAPPING PIN FOR NCT5563D				
PIN	5563D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	24M_48M_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE
21	TESTMODE1_EN	SOUTA	DISABLE TESTMODE	ENABLE TESTMODE



	R350	R329	R357	R309	C354
5562D	o	X	o	o	X
5563D	o	o	o	o	o

**2015.6.8 remove R343 R350**

**2015.6.11 remove R363 R357**



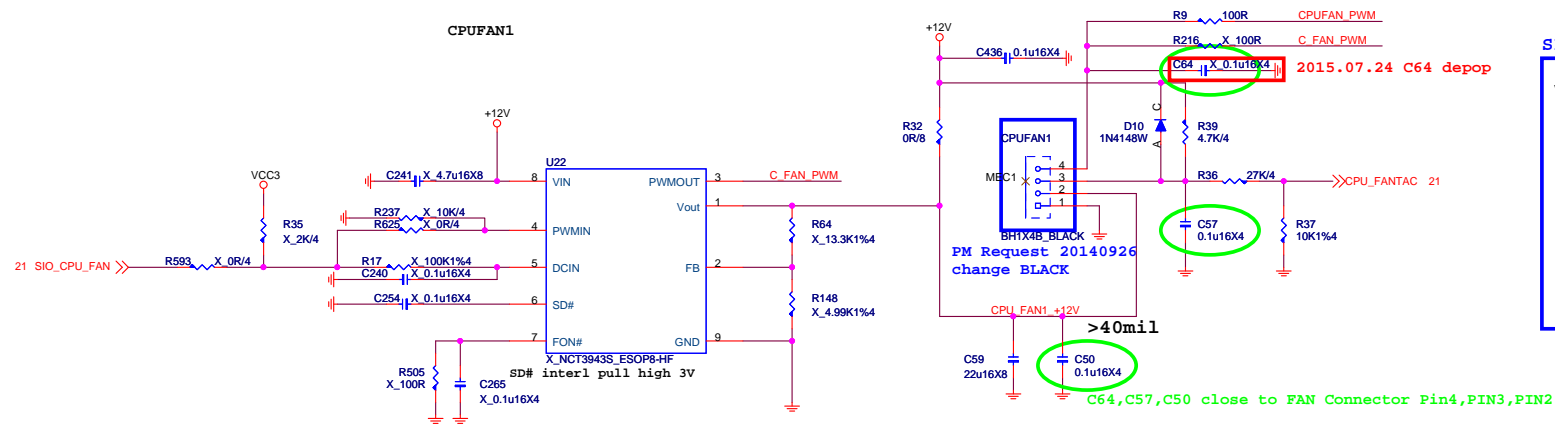
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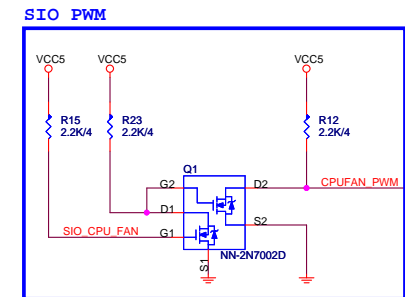
## Type G : 4 PIN CPU FAN FROM SIO



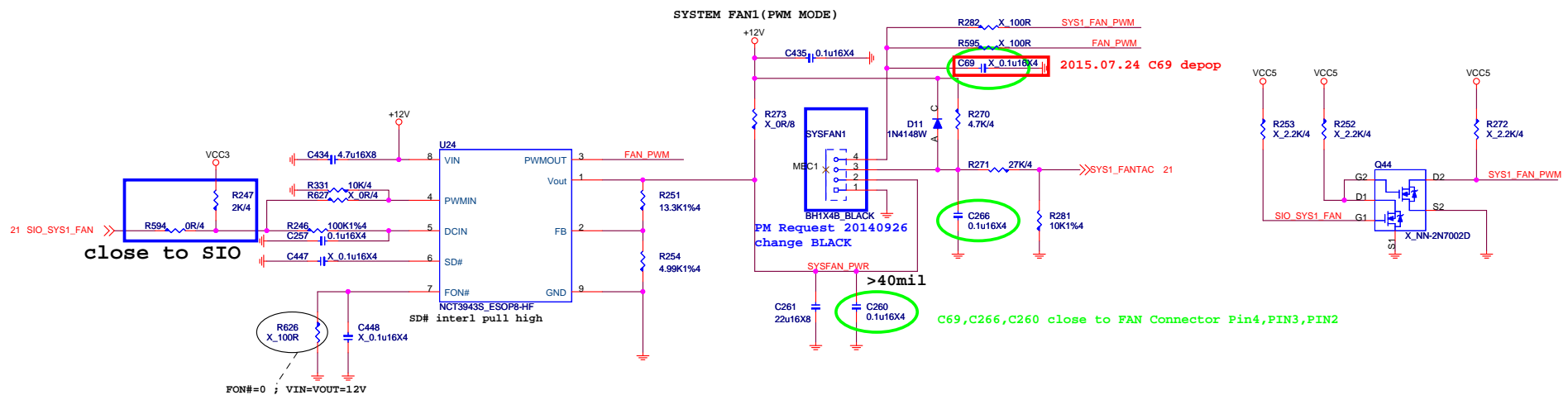
```

CPUFAN_PWR_OFF
GPIO Control
Deafult GPI
If USE CUT POWER
1.OPEN DRAIN LOW:SD# LOW  Active , CPUFAN(PIN2)= 0V
2.OPEN DRAIN : SD# Internal Pull high , CPUFAN(PIN2)=12V

```



**Type H : 4 PIN SYS FAN FROM SIO**



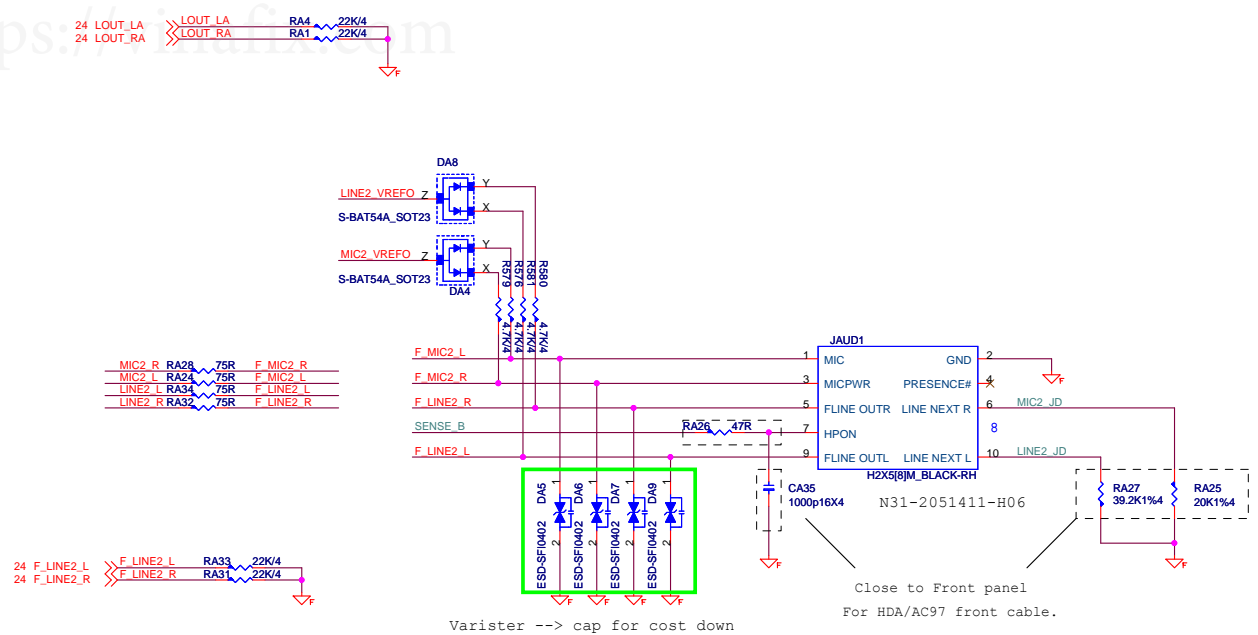
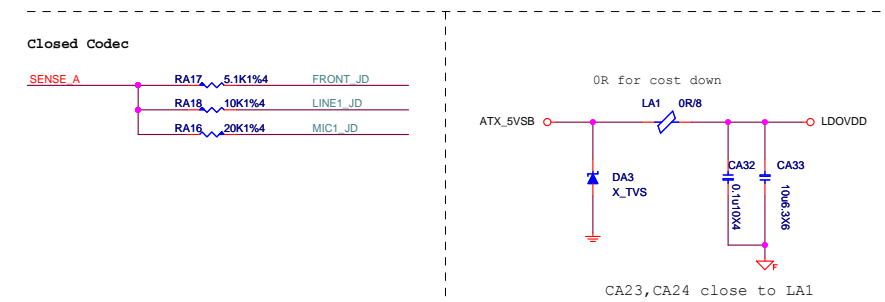
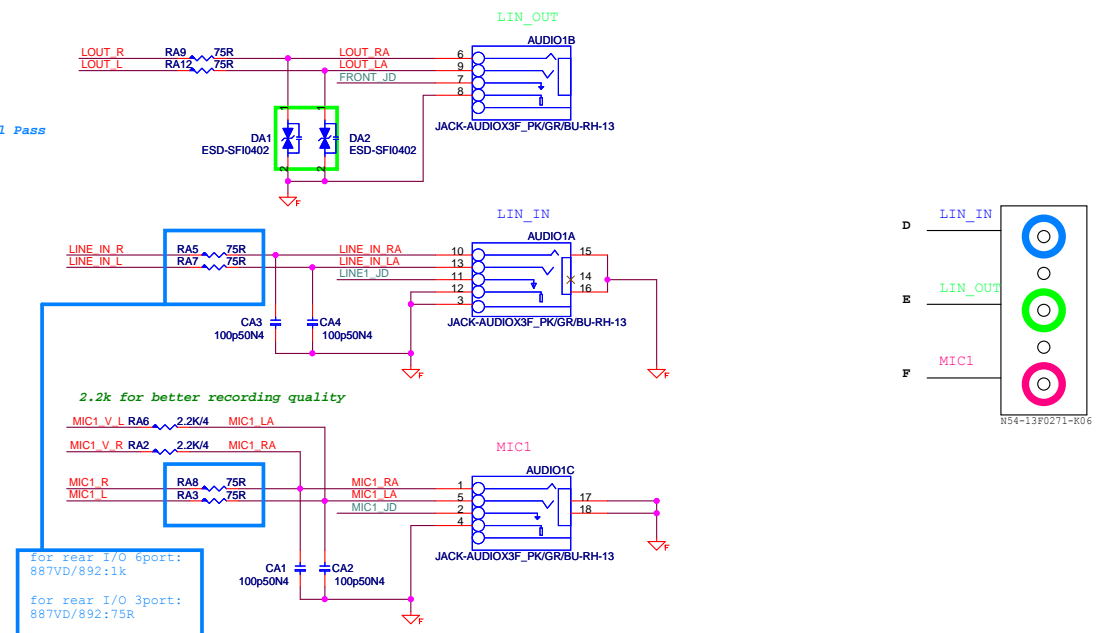
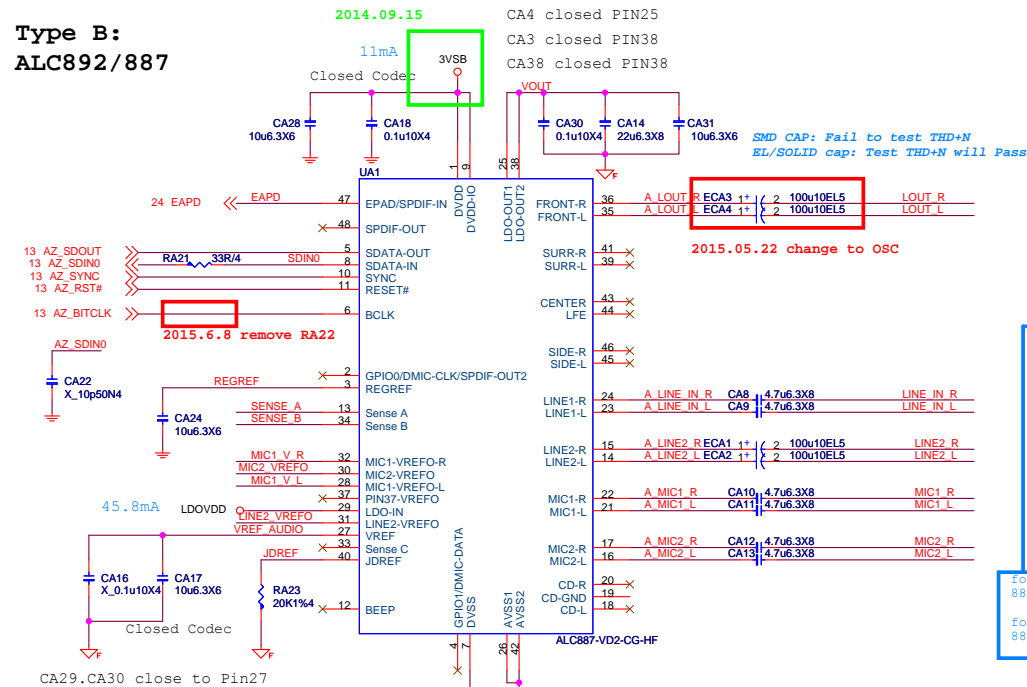
**MICRO-STAR INT'L CO.,LTD**

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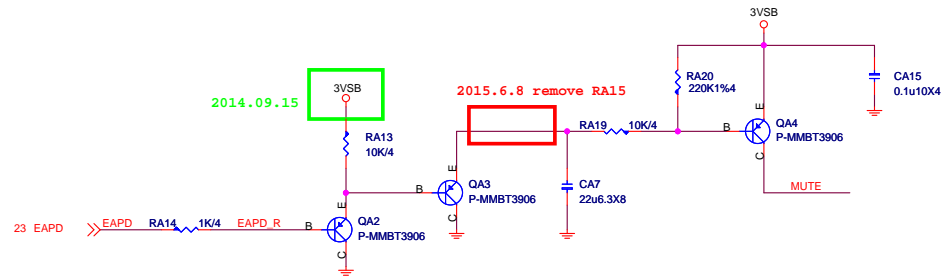


Type B:  
ALC892/887



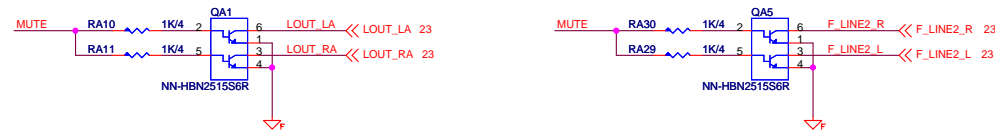
# Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog



<https://vinafix.com>

Vinafix.com

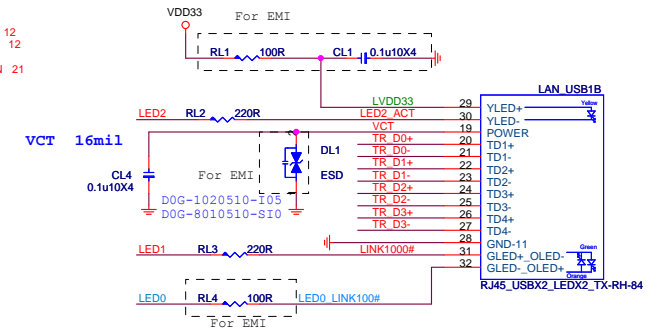
History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

# RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09  
8111G:B06-081116C-R09

## LAN Connector



Pin33: 4 via from top layer to GND layer  
and make the via at the center of IC.

<https://vinafix.com>

### 8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

### 8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



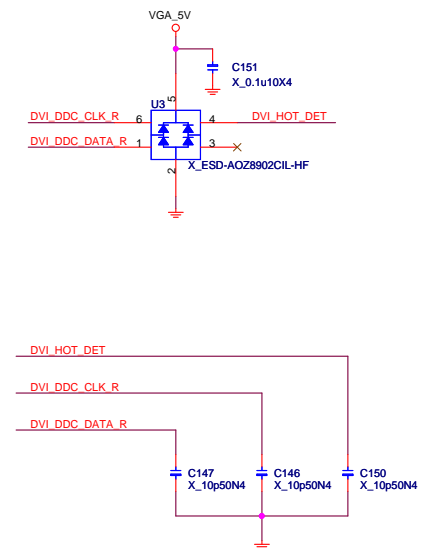
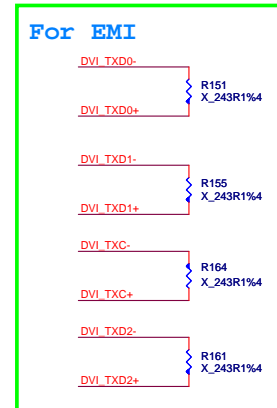
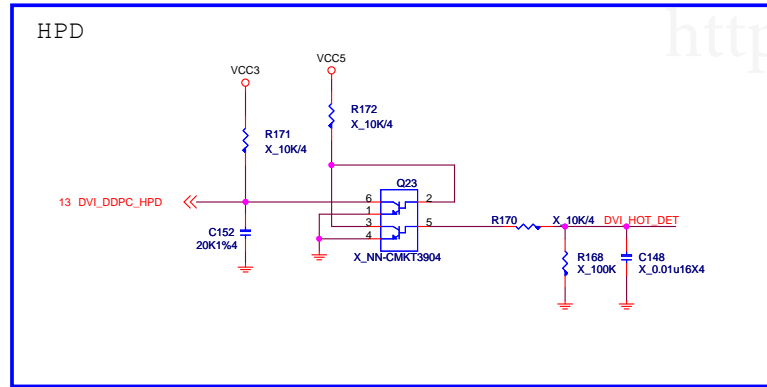
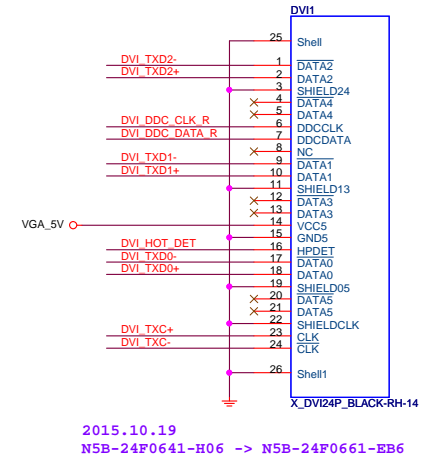
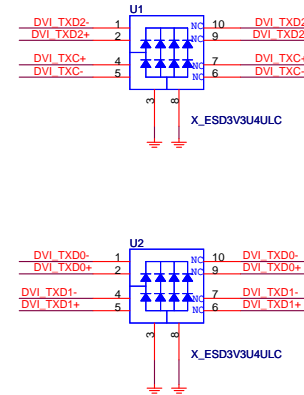
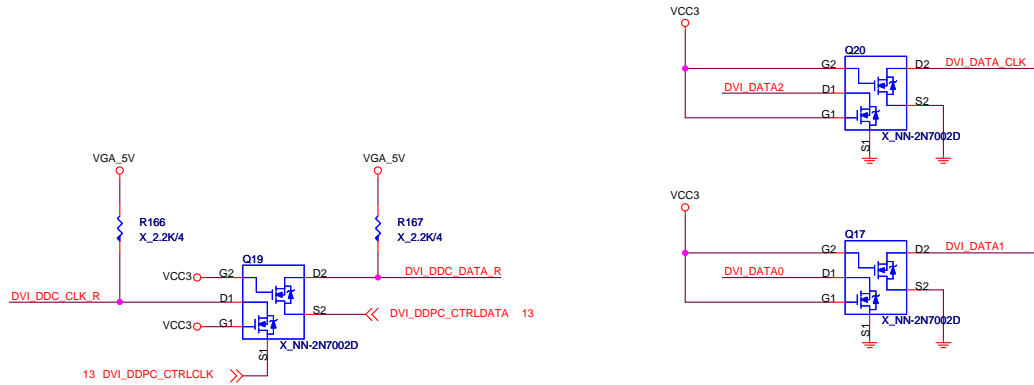
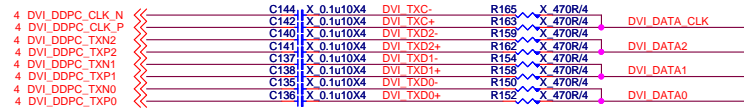
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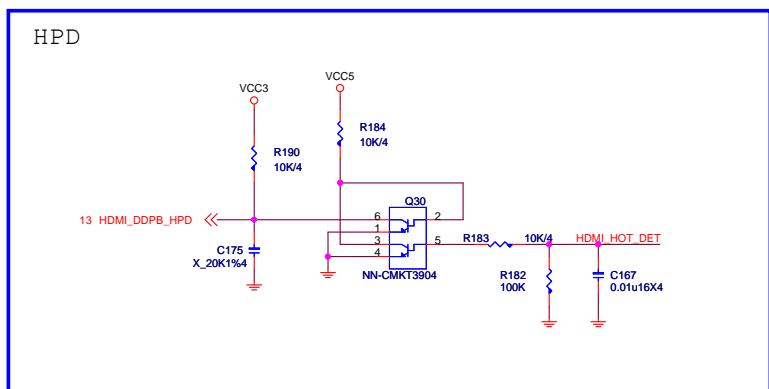
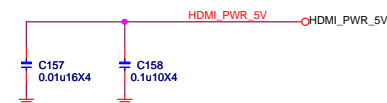
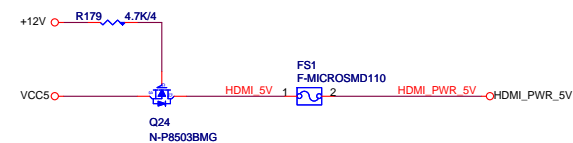
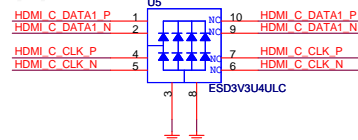
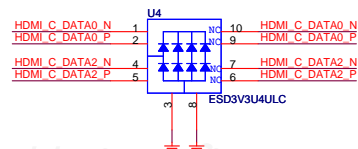
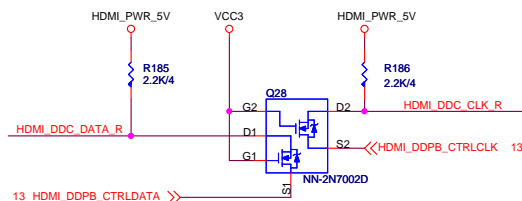
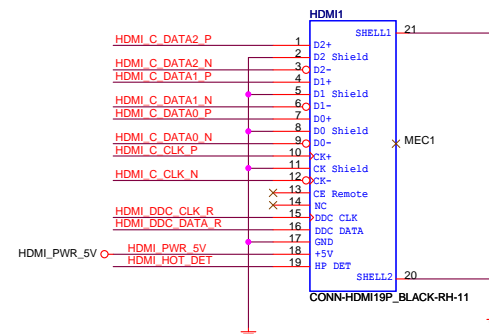
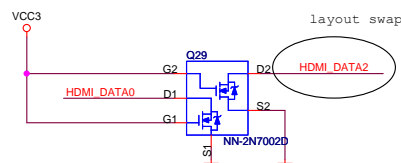
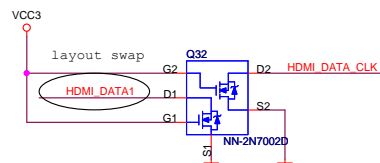
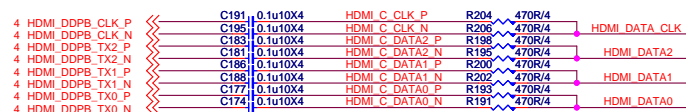
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# DVI level shifter

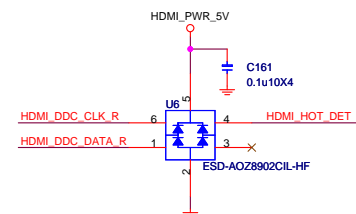
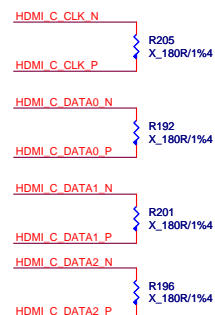
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

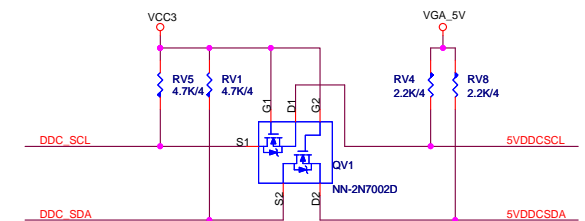
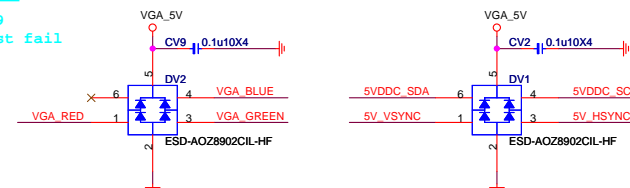
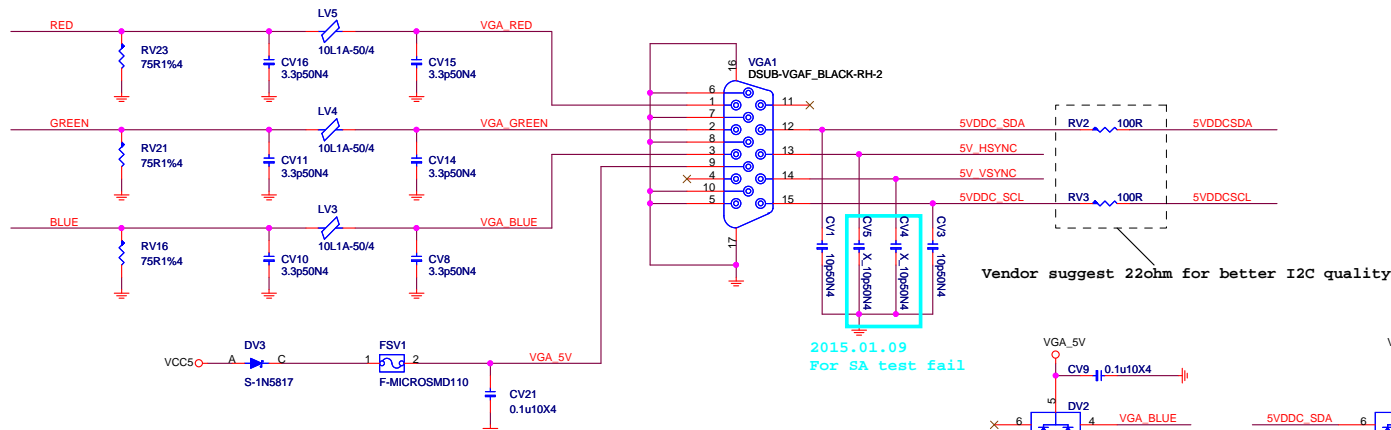
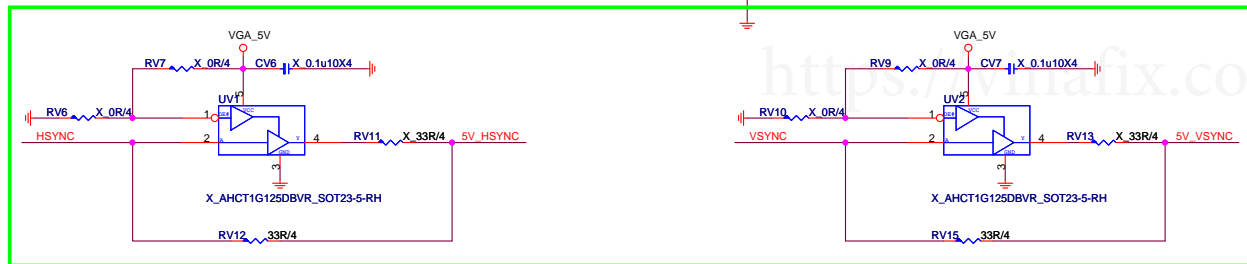
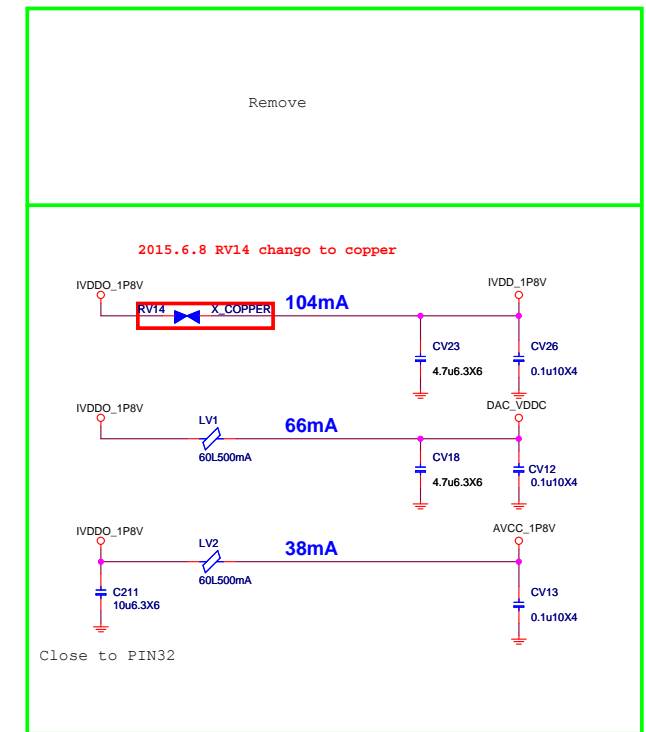
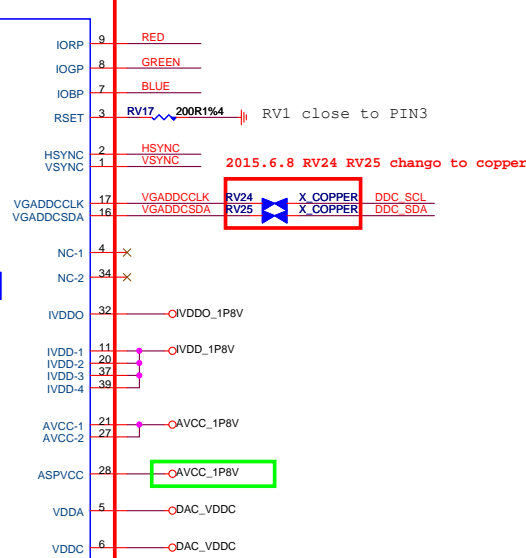


For EMI



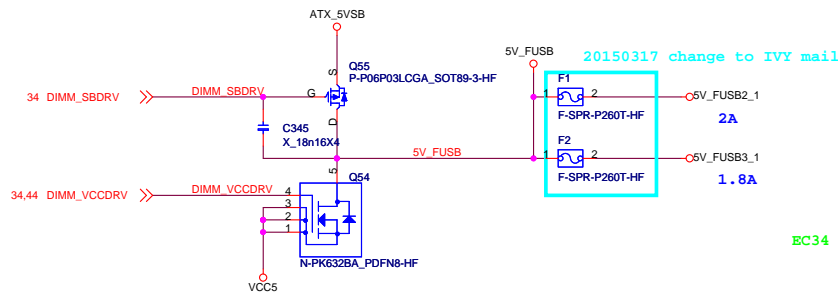
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

Timing diagram for DP\_TX0 and DP\_TX1 signals. The diagram shows two differential signal pairs, DP\_TX0 and DP\_TX1, each with a period of 100 ns. The signals are shown as differential pairs with a common-mode voltage of 1.00V. The signals are labeled DP\_TX0\_P and DP\_TX0\_N for the first pair, and DP\_TX1\_P and DP\_TX1\_N for the second pair. The signals are shown as differential pairs with a common-mode voltage of 1.00V. The signals are labeled DP\_TX0\_P and DP\_TX0\_N for the first pair, and DP\_TX1\_P and DP\_TX1\_N for the second pair. The signals are shown as differential pairs with a common-mode voltage of 1.00V. The signals are labeled DP\_TX0\_P and DP\_TX0\_N for the first pair, and DP\_TX1\_P and DP\_TX1\_N for the second pair.



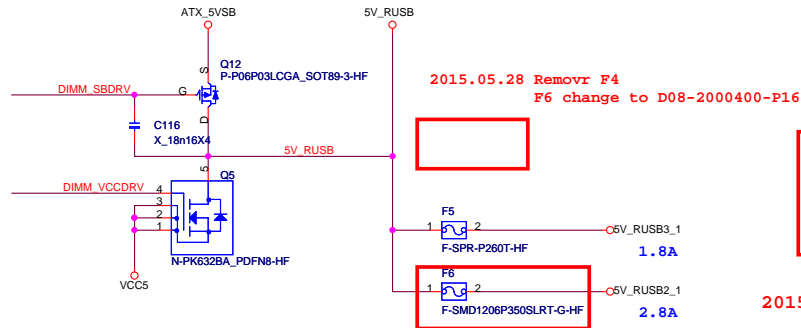
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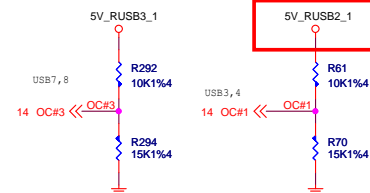
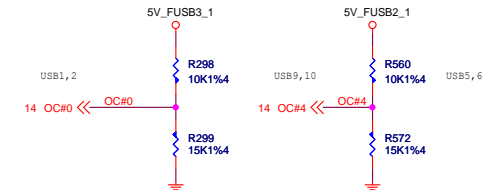


EC34 -> 560uF

2015.05.28 Remove USB CAP EC33

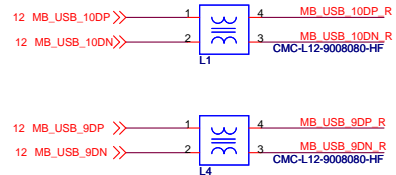


2015.05.28 Remove USB CAP EC3

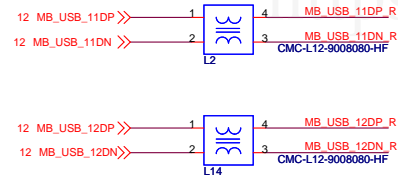


2015.05.28 change to 5V\_RUSB2\_1  
2015.06.08 Remove R559,R575 and R605,R409

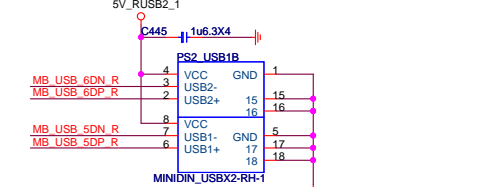
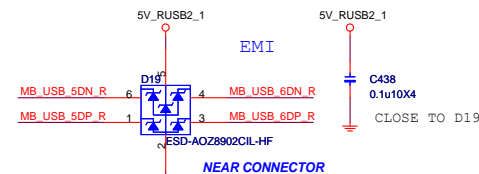
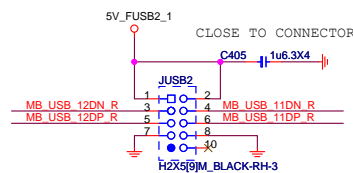
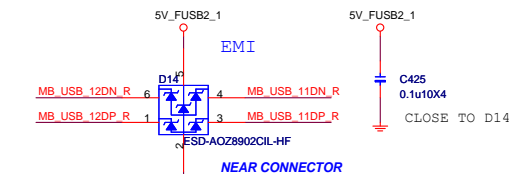
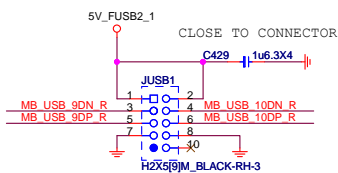
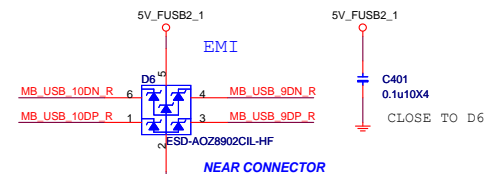
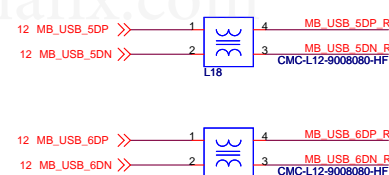
#### FRONT USB PORT 9,10



#### FRONT USB PORT 11,12



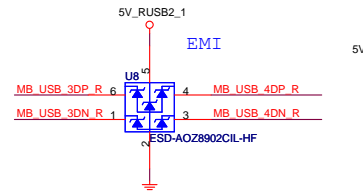
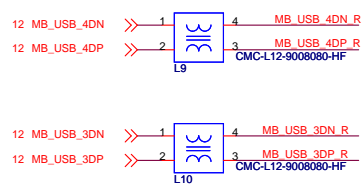
#### REAR USB PORT 5,6



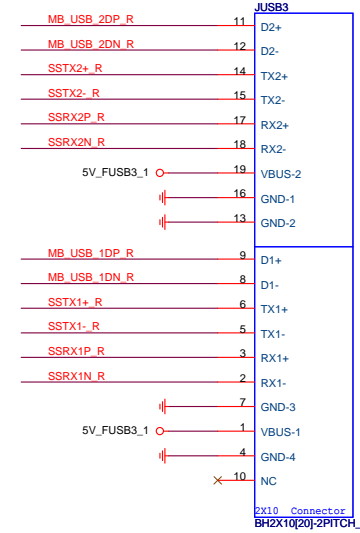
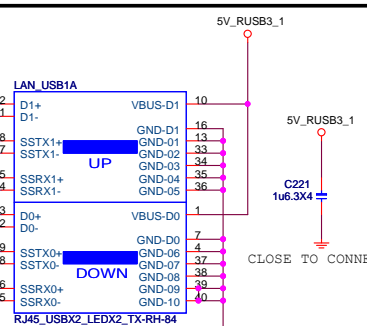
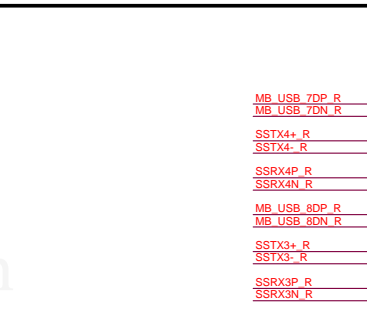
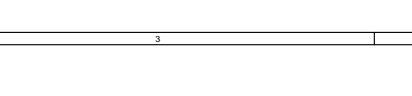
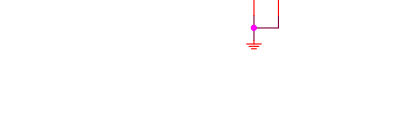
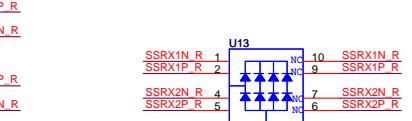
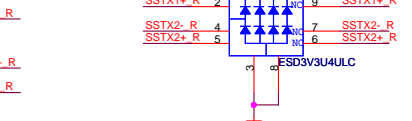
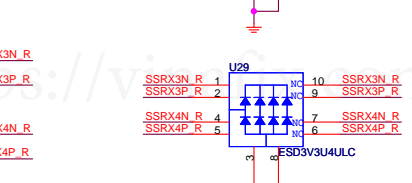
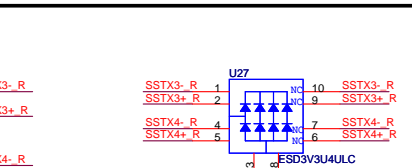
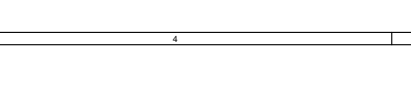
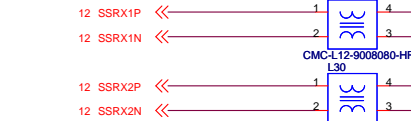
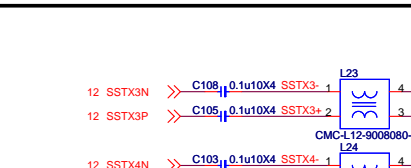
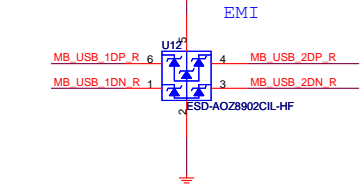
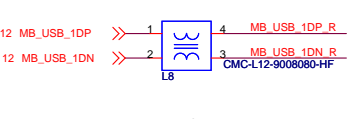
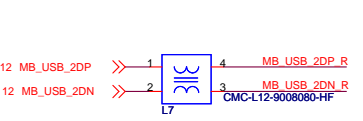
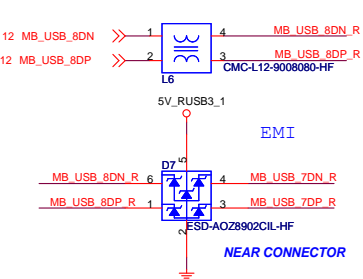
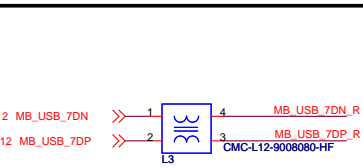
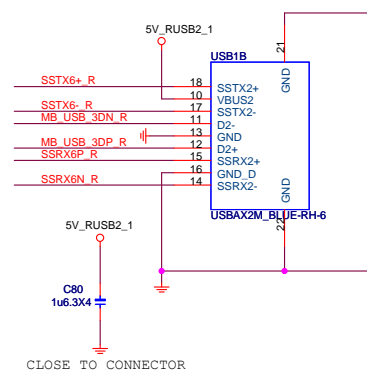
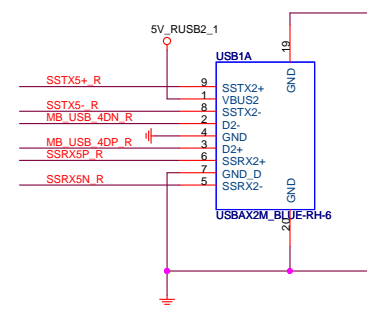
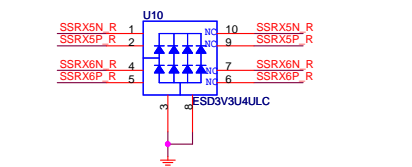
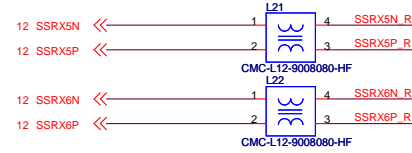
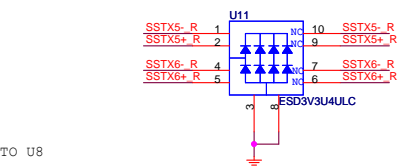
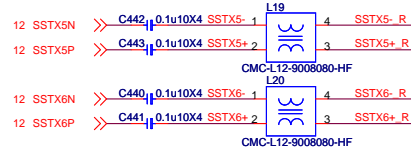
2015.05.22 JUSB2 change to USB11,12  
PS2\_USB change to USB5,6


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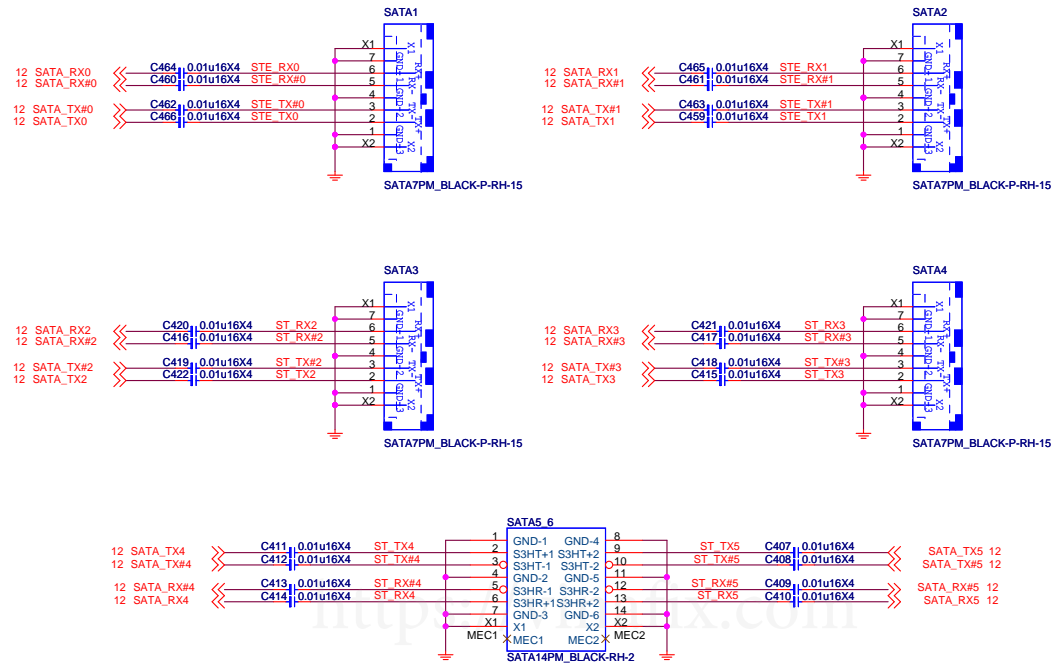




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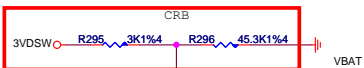
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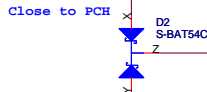
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Custom	SATA connector	13
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CUT\_VBAT

2015.7.20 R295,R296 change to POP

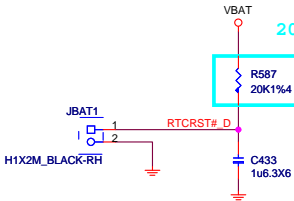
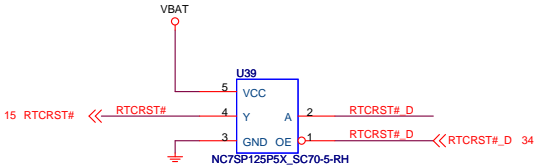


Close to PCH

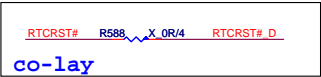


2015.6.1 add VBAT1 in bottom side

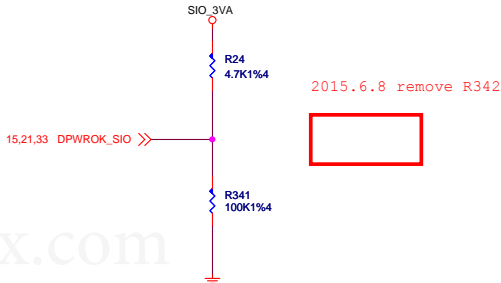
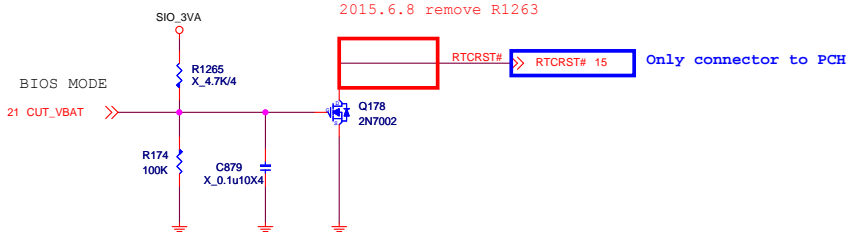
tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z



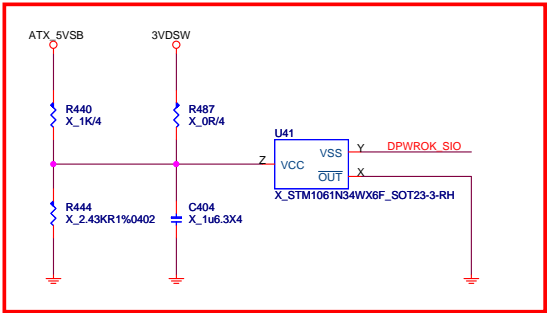
2014.12.29



co-lay



2015.6.10 add circuit

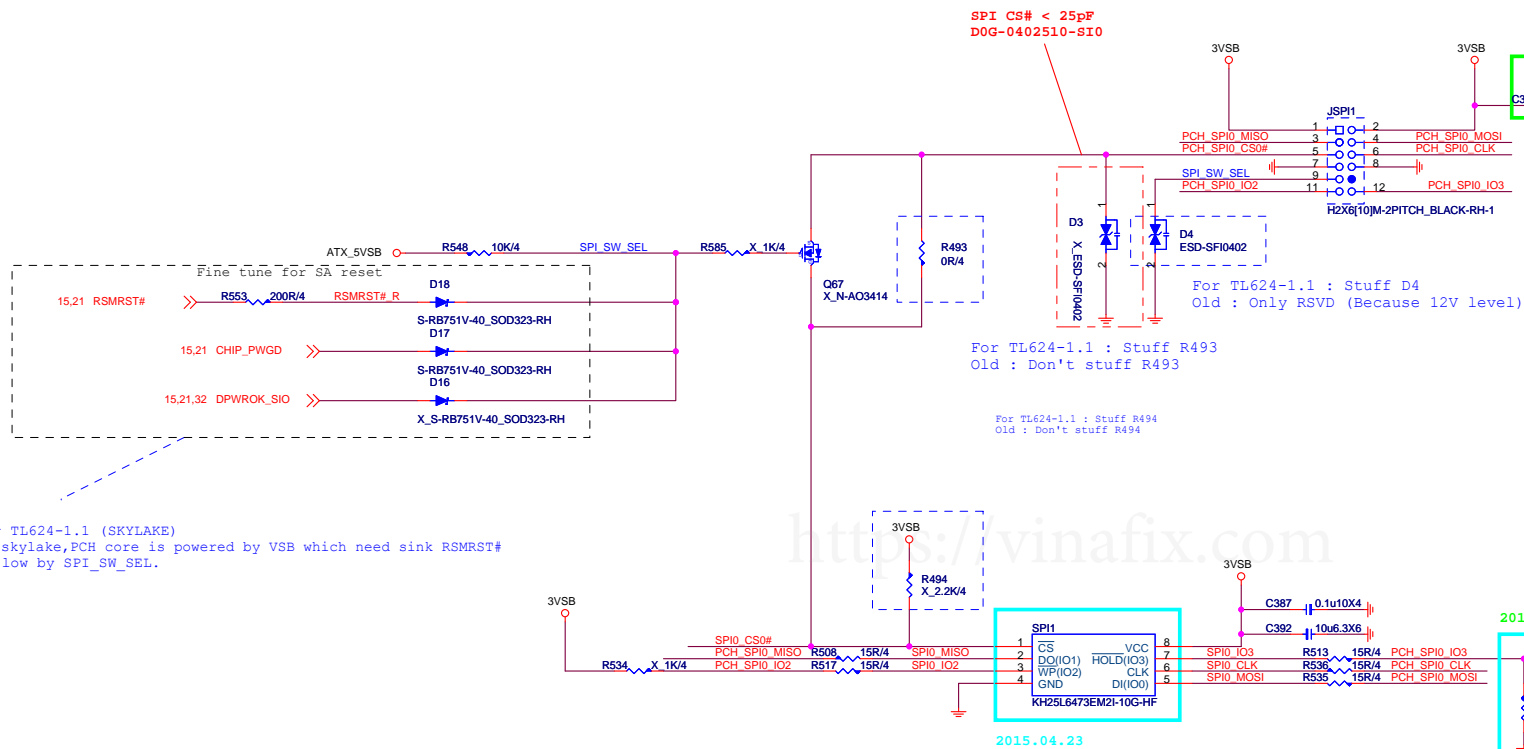


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15 PCH\_SPI0\_MOSI << PCH\_SPI0\_MOSI  
15 PCH\_SPI0\_MISO << PCH\_SPI0\_MISO  
15 PCH\_SPI0\_CLK << PCH\_SPI0\_CLK  
15 PCH\_SPI0\_CS0# << PCH\_SPI0\_CS0#  
15 PCH\_SPI0\_IO2 << PCH\_SPI0\_IO2  
15 PCH\_SPI0\_IO3 << PCH\_SPI0\_IO3



For TL624-1.1 (SKYLAKE)  
In skylake, PCH core is powered by VSB which need sink RSMRST#  
to low by SPI\_SW\_SEL.

- \* if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
- \* if you support Standby power in S5 Status(Ex; PCH is B75 Chipset), component Q14.G Pull-high to ATX\_5VSB, Q14 must select "Vth" under 1V (Component Suggestion as below)

D03-0341409-A68 / D03-0230019-A30

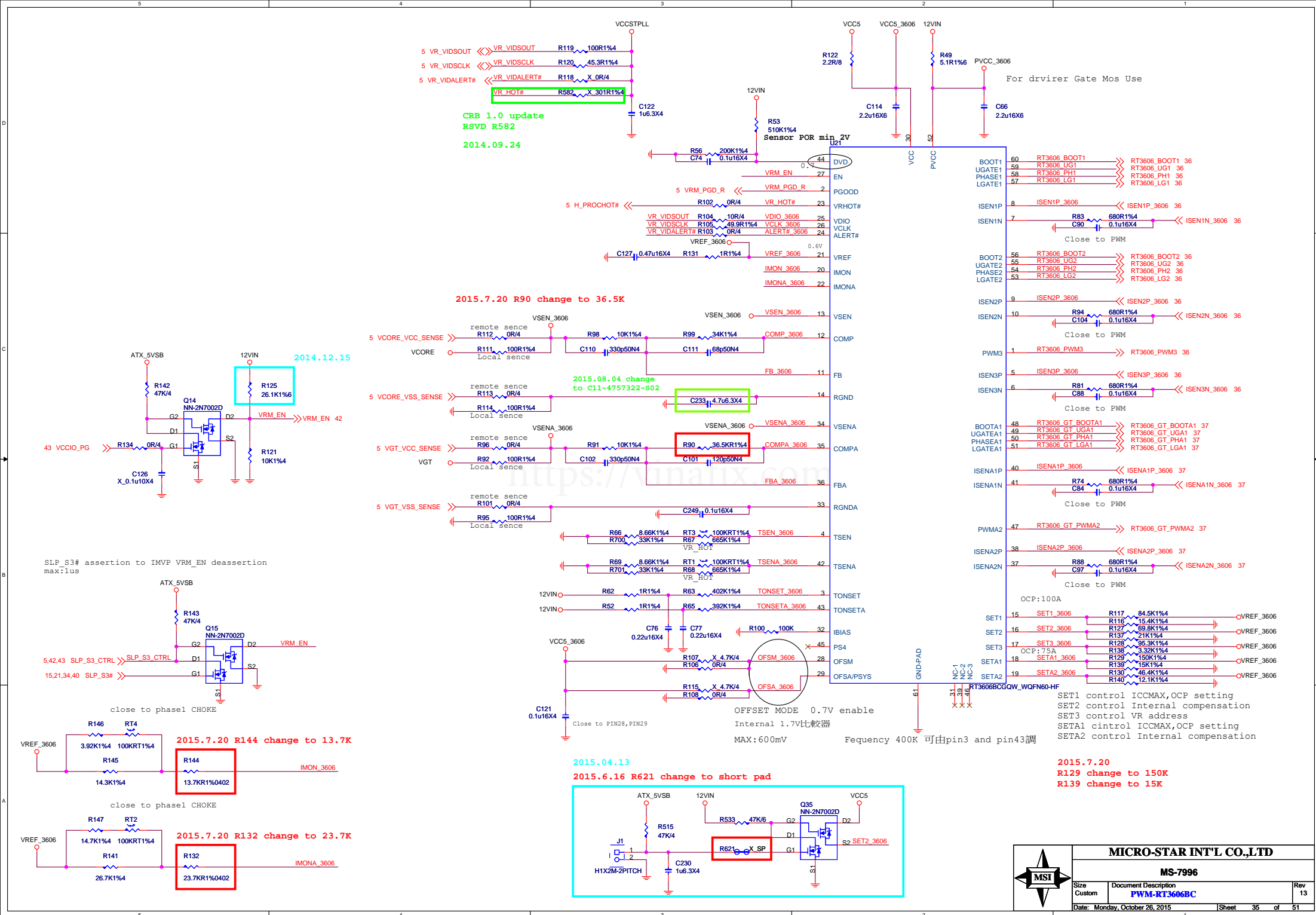


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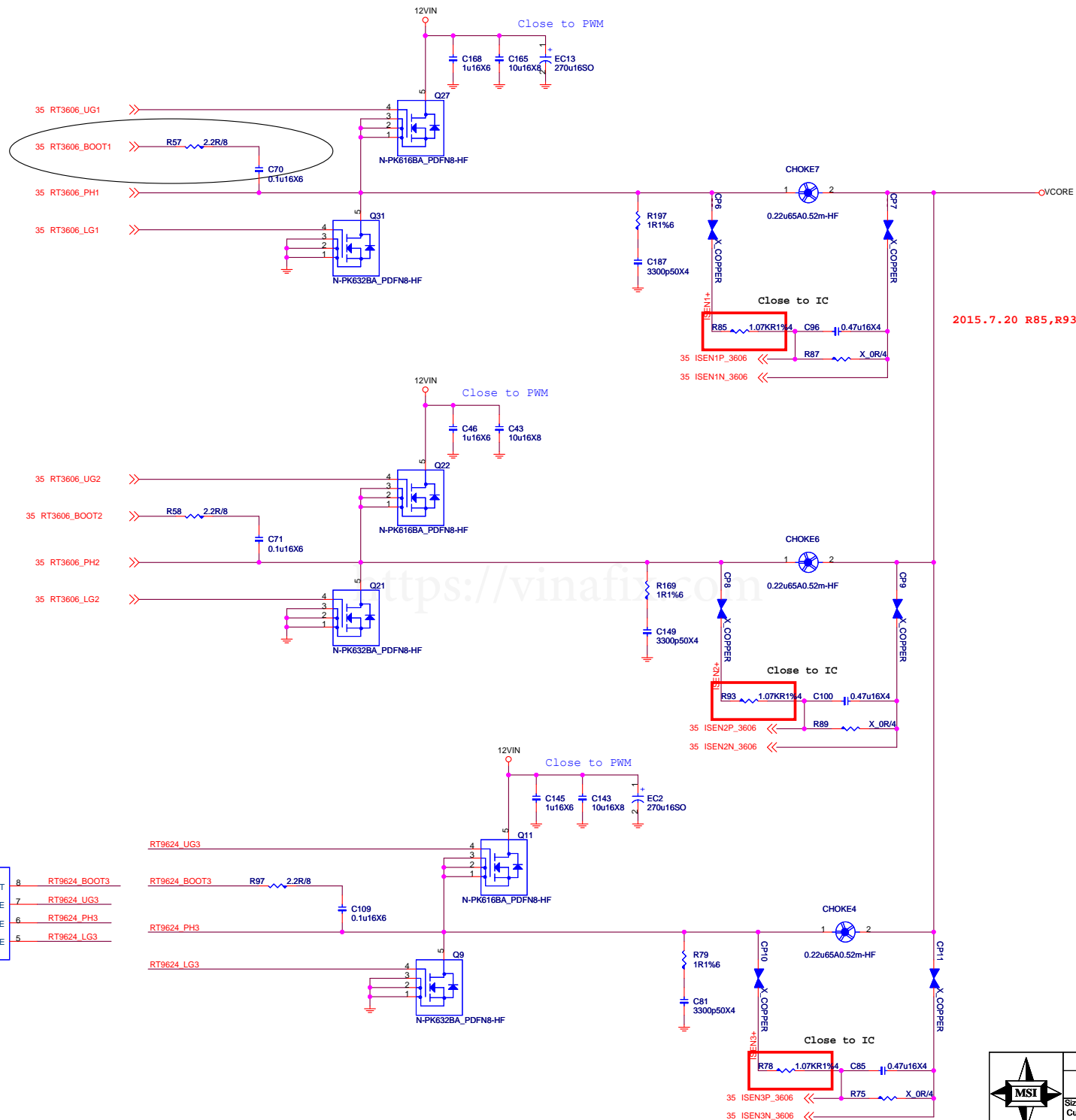
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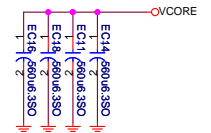


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ICCMAX: 79A  
LL: 2.1m ohm

2015.7.20 R85, R93, R78 change to 1.07K

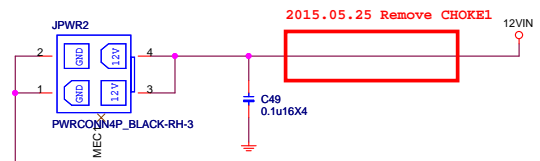


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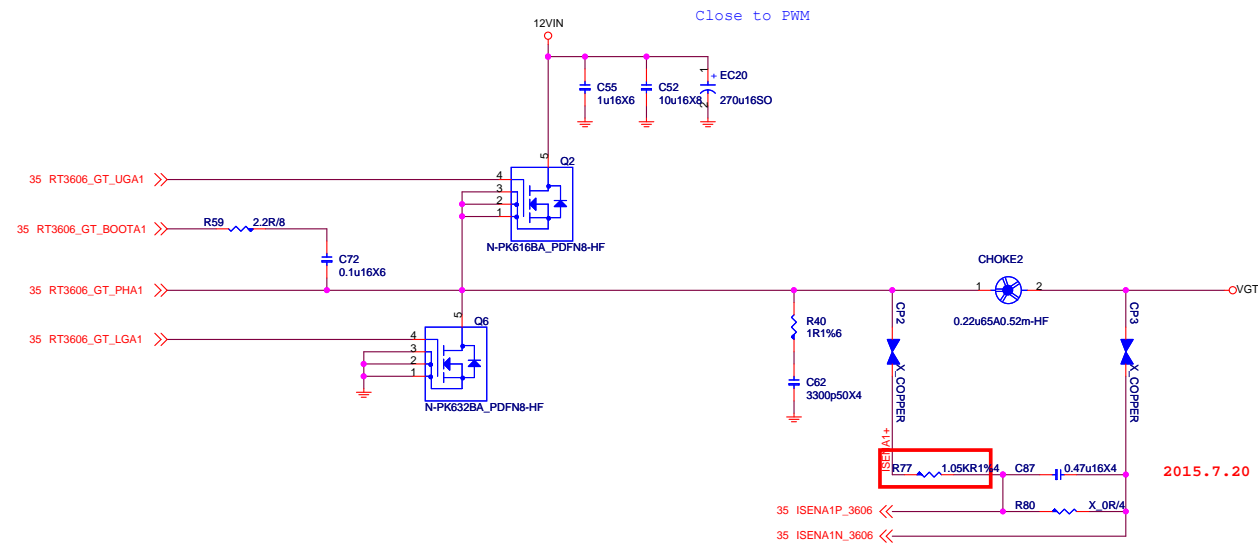
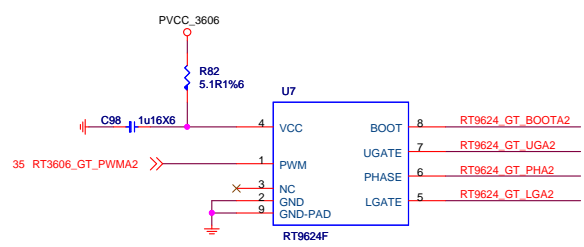




2015.05.25 Remove CHOKEL

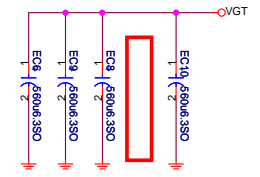


2015.09.17 Remove L42

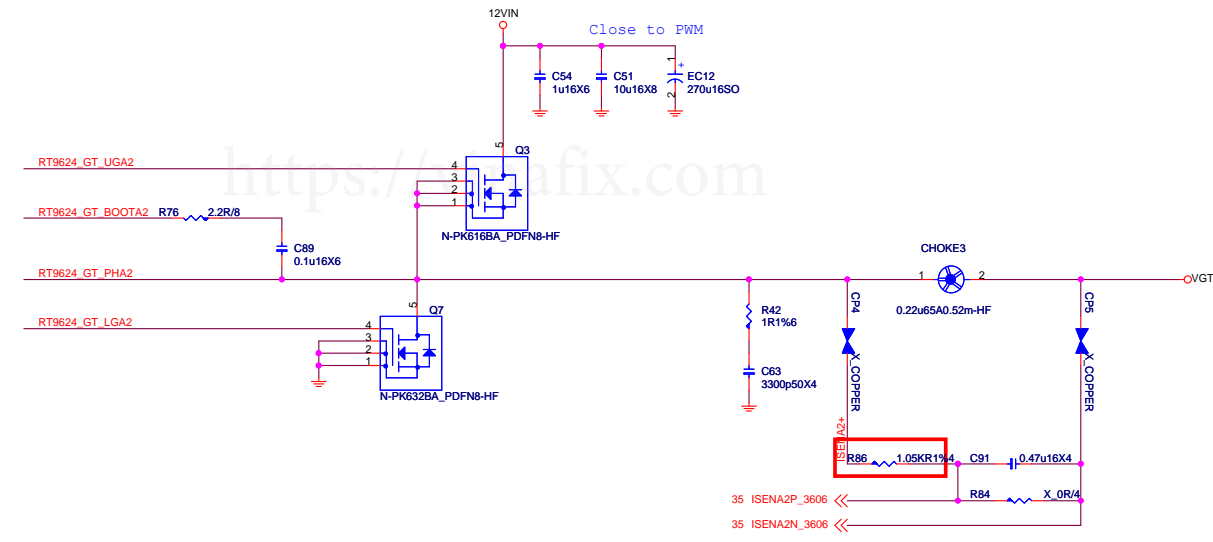


ICCMAX:51A  
LL:3.1m ohm

2015.7.20 R77,R86 change to 1.05K



2015.6.9 remove EC7



MICRO-STAR INT'L CO.,LTD			
MS-7996			
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Custom	VGT(P-PAK) PHASE1-2	13	
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DDR4\_1.2V 2.8A+ 4.75A+0.375A=7.925

2.8A FOR CPU  
4.8A FOR 2DIMM DDR4  
0.375A FOR VTT\_DDR

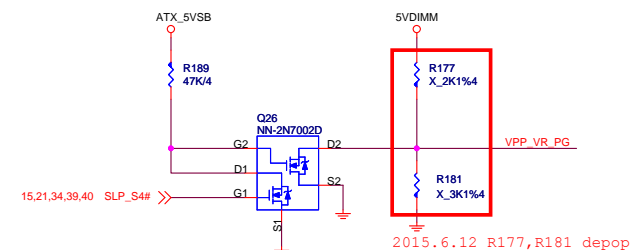
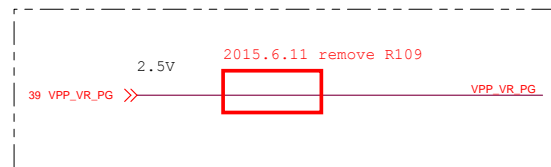
OCP = 7.925A\*1.5=11.8875A

Current limit= 95.3K(R1054)\*5uA/10/4mohm)=11.91A

2015.05.22 change to DDR4

VID	Reference Voltage (V)
H	0.675
L	0.75

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))} \\ &= 9.357 * 0.44 \\ &= 4.154A \end{aligned}$$

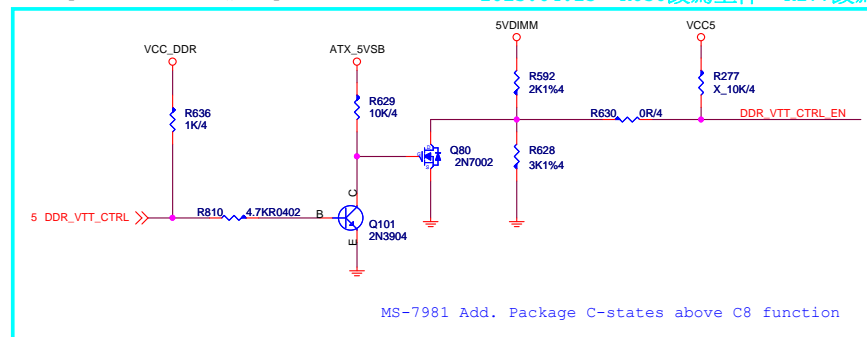


2015.6.11 remove circuit



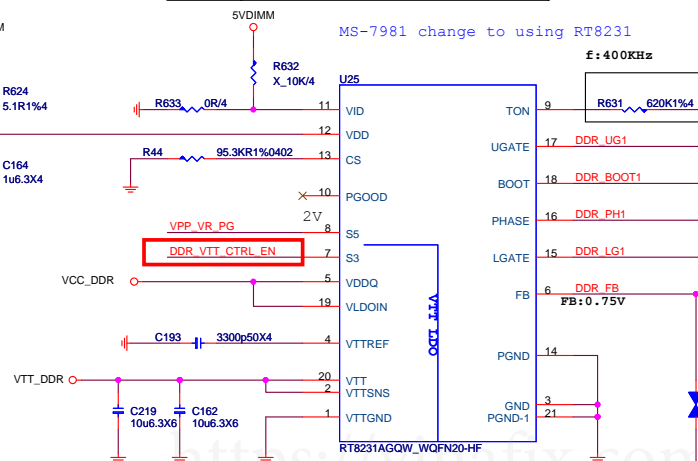
SLP\_S4# de-assertion to VDDQ ramp down start

VPP ramp down after VDDQ ramp down



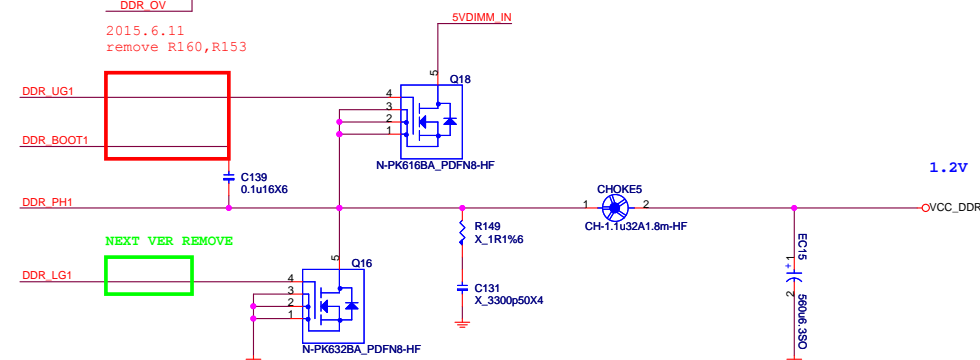
MS-7981 Add. Package C-states above C8 function

MS-7981 change to using RT8231



MAX: 7.925A

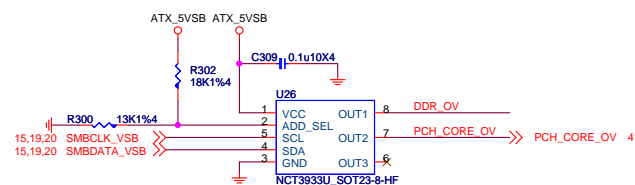
1.2V



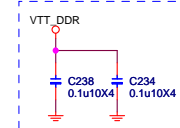
1.2V

### UPI VOLTAGE CONSOLE

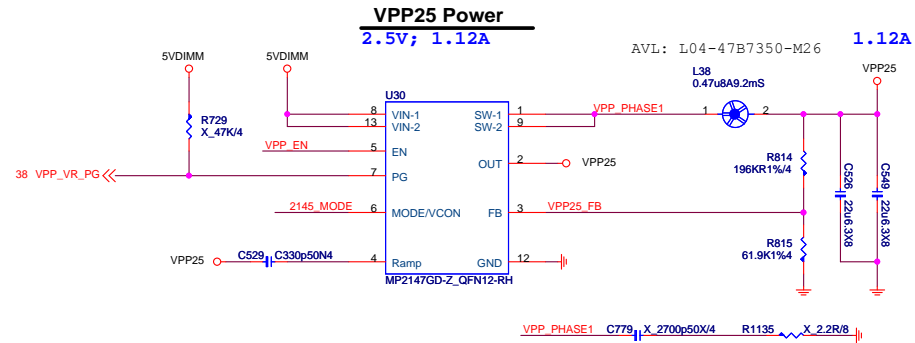
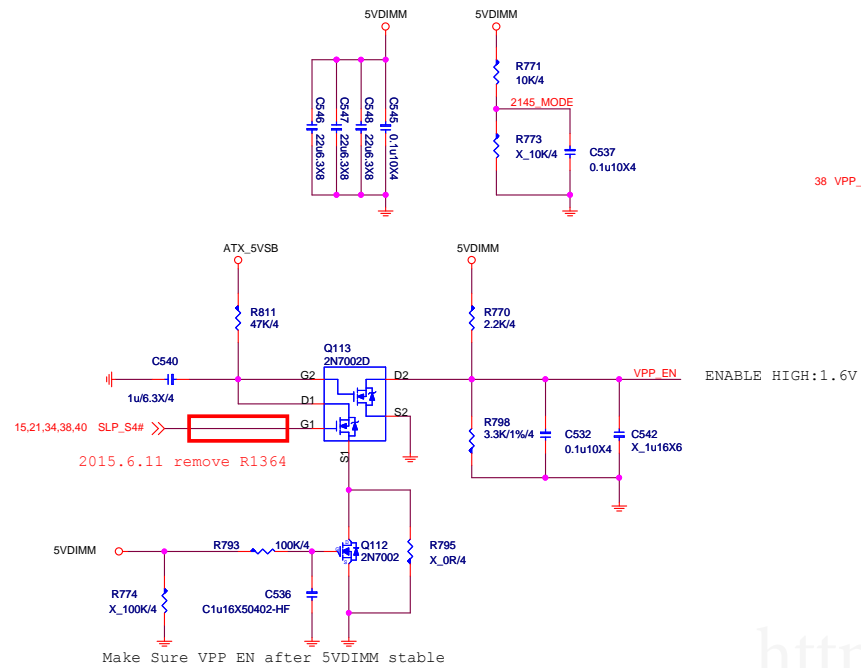
0x26:RH=18K,RL=13K



0.1uFx1 per dimm



2DIMM :1.12A FOR DDR VPP2.5V



**MICRO-STAR INT'L CO.,LTD**

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For Cost down VCCST&VCCPLL merge



# PCH 1VSB

1.0V; 7.858A

OCp = 11.787A

Rocset =  $1.5 * I_{max} * R_{dson}(low) / I_{ocset}$   
 =  $1.5 * 7.858 * 5mohm / 10uA$   
 = 5.8935K

Rocs: 5.9K, OCp:

D03-4C05N03-005 : 11.8A

D03-632BA0C-N03 : 12.82A

use UBIQ MOS need Check

Rdson(low) 4.5V

D03-4C05N03-005 : 5 mohm

D03-632BA0C-N03 : 4.6mohm

D03-3056M00-U47 : 6.2mohm

2015.04.23 change to UP1540

2014.08.22 close to U34

2015.01.22  
 for up1540:stuff R438->36K,  
 C379->NC, C373->3.3nF  
 for RT8125:R438.C379.C373->NC

2015.01.22  
 for up1540:R403->2.2R, C362->1uF  
 for RT8125:R403->10R, C362->1uF

$$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

MAX:10.664A

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out\_max})) * (V_{out}/V_{in})$$

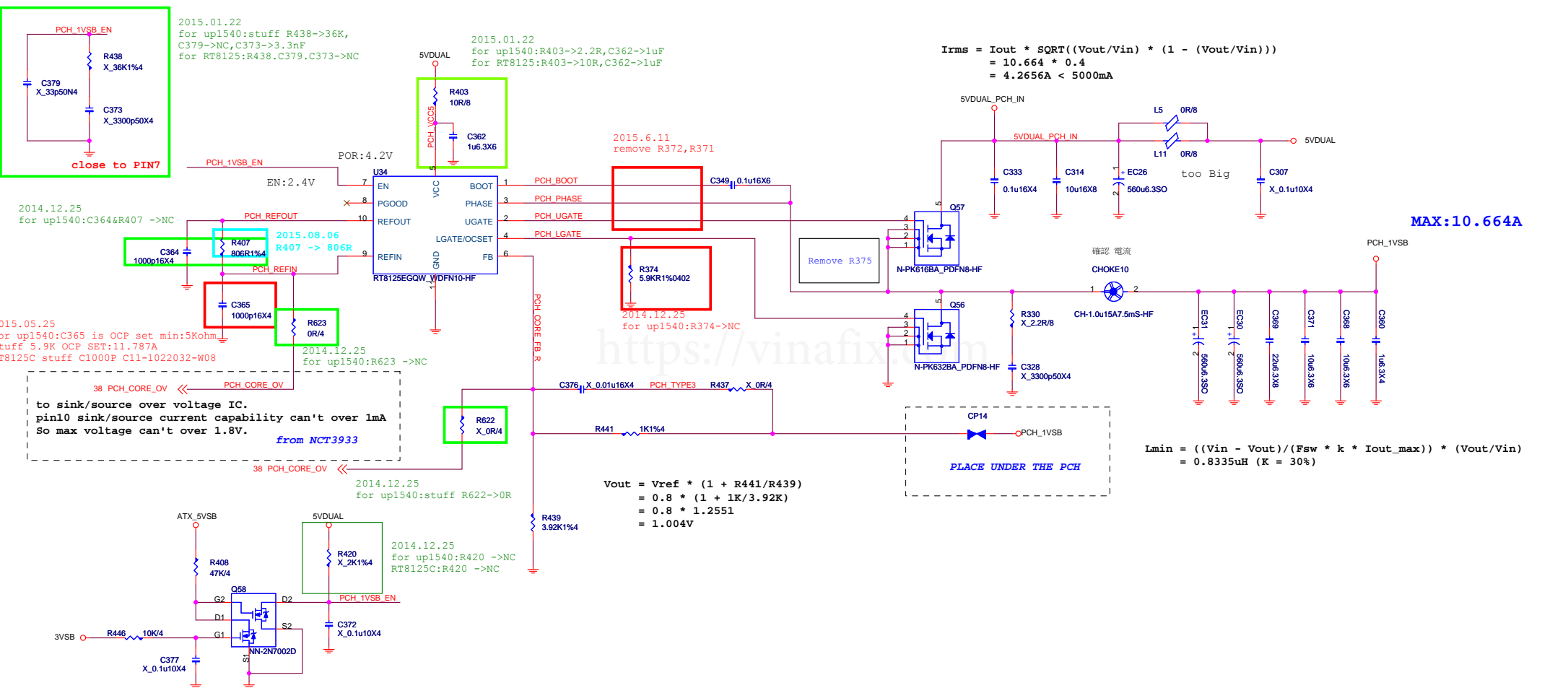
$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{441}/R_{439})$$

$$= 0.8 * (1 + 1K/3.92K)$$

$$= 0.8 * 1.2551$$

$$= 1.004V$$



**SA Power:1.05V,11.1A**

$$OCP = 11.1A * 1.4 = 15.54A$$
$$R_{ocs}(R15) = OCP * R_{dson}(\text{Low side}) 3.4\text{mohm}] / 10\mu A$$
$$= 15.54 * (3.4) \text{ mohm} / 10 \mu\text{A}$$
$$= 5.2836 \text{ Kohm}$$

Rocs:5.2836K,OCP:

D03-4C05N03-005 : 15.76A

D03-632BA0C-N03 : 16.24A

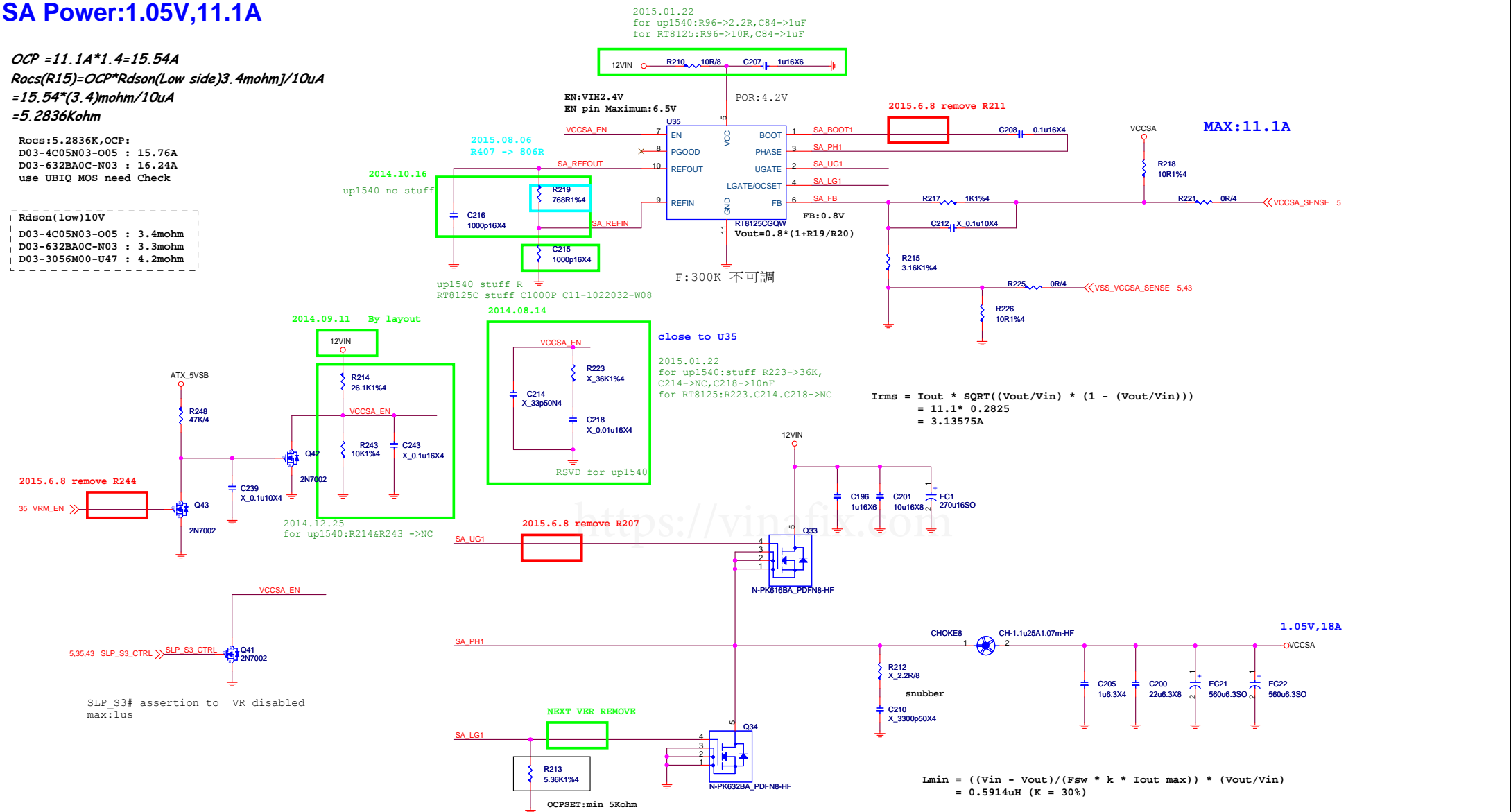
use UBIQ MOS need Check

Rdson(10V)

D03-4C05N03-005 : 3.4mohr

D03-632BA0C-N03 : 3.3mohr

D03-3056M00-U47 : 4.2mohm



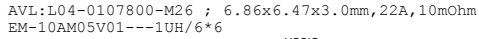
**MICRO-STAR INT'L CO.,LTD**

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Size Custom	Document Description <b>VCCSA - POWER RT8125E</b>	Rev 13
Date: Monday, October 26, 2015		Sheet 42 of 51

0.95V; 5.5A

*ILIMIT=8.5~9A*

VCCIO

MAX: 5.5A

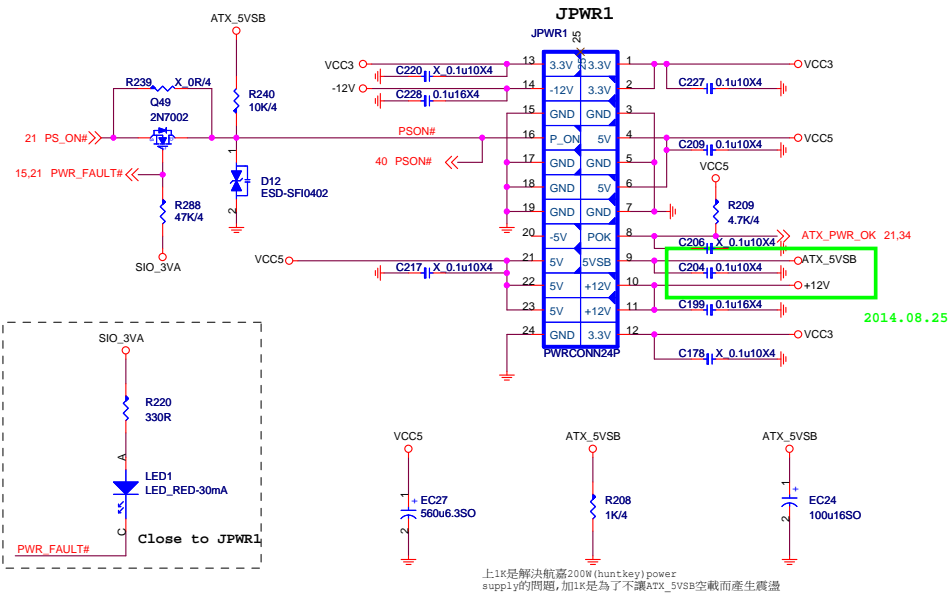
2014.12.17

Vinafix.com

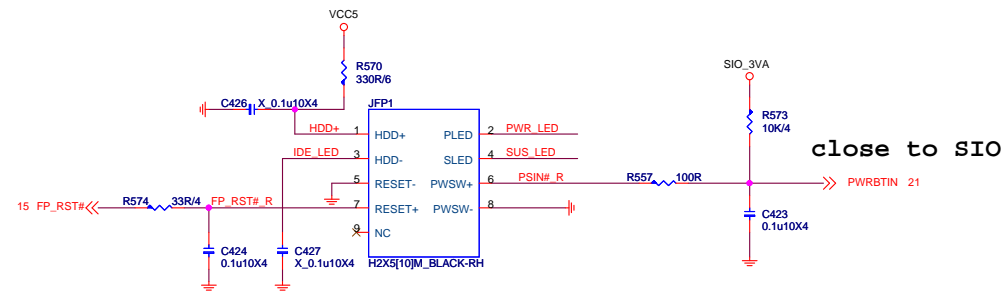
**MS-7996**

Size Custom	Document Description <b>VCCIO - POWER NB671</b>	Rev 13
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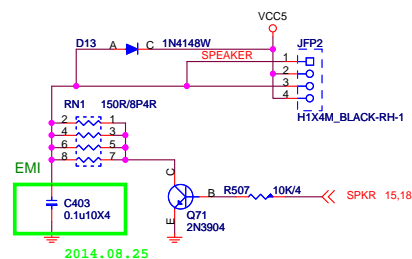
## ATX POWER CONNECTOR



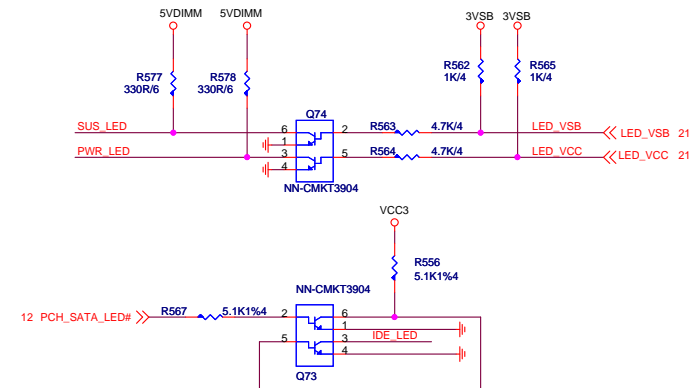
## FRONT PANNEL



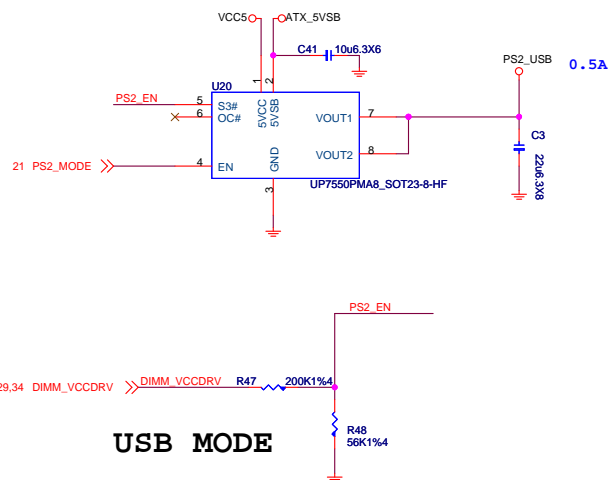
## Speaker Pin Header



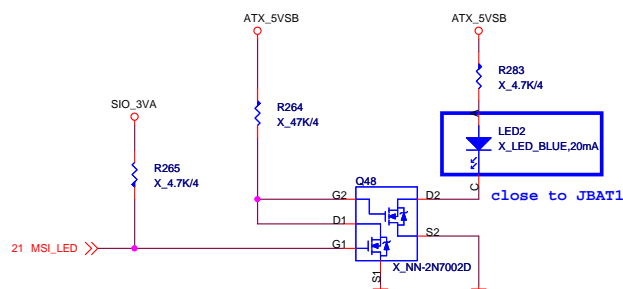
## LED ( for NV5533)



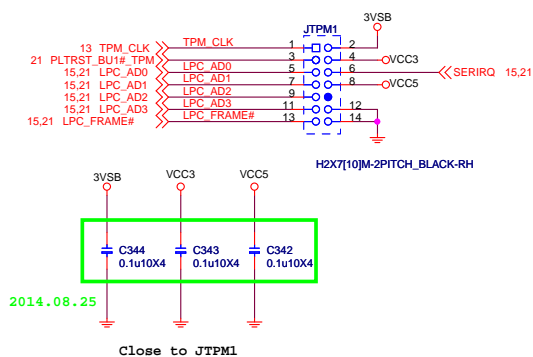
## PS2 POWER



## MSI LED

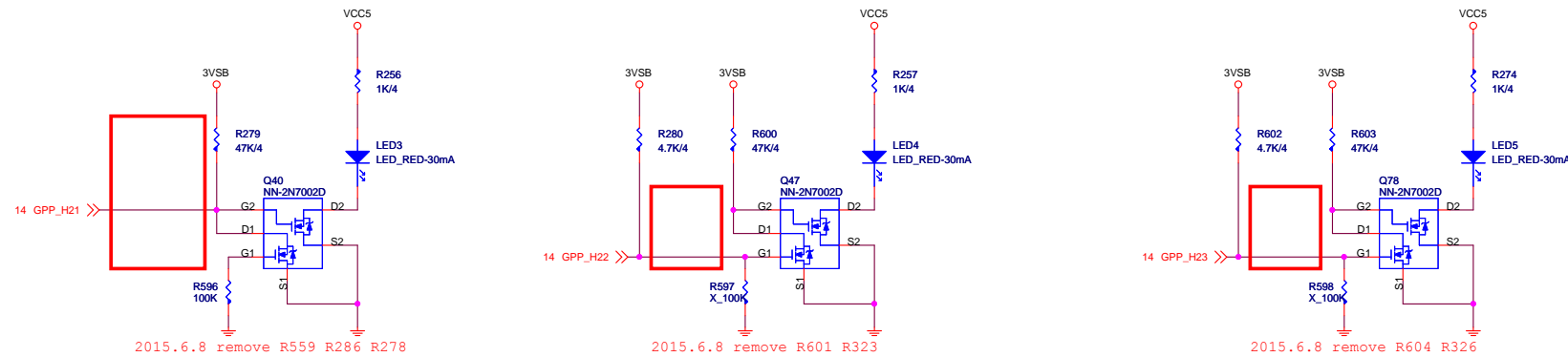


## TPM





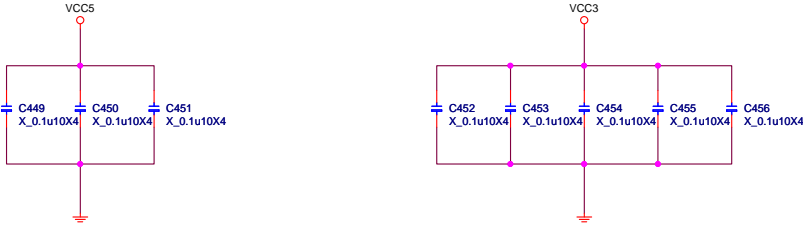
DEBUG LED



GPIO LED	GPP_H21	GPP_H21	GPP_H21
	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
亮			
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

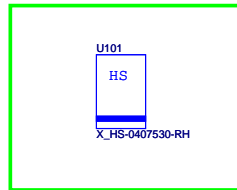
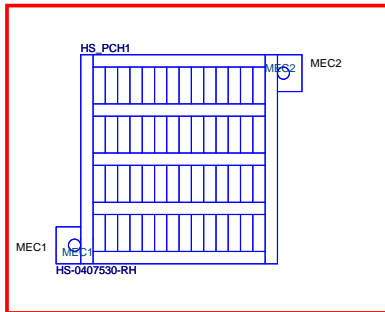
- 關機斷電狀態下，3個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
  2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
  3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
  4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

EMI CAP

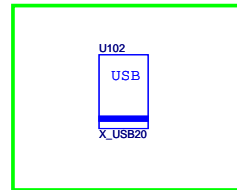


<https://vinafix.com>

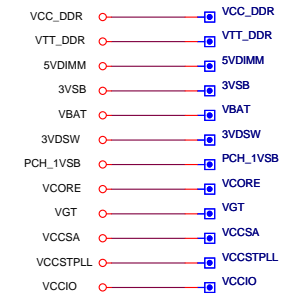
2015.06.01 change to using E31-0407530-K08



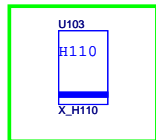
2015.08.03  
colay Heatsink for H110



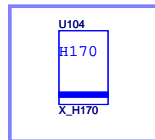
2015.08.03  
USB2.0 Connector colay for H110



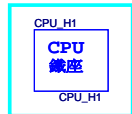
2015.08.03  
PCH H110 colay



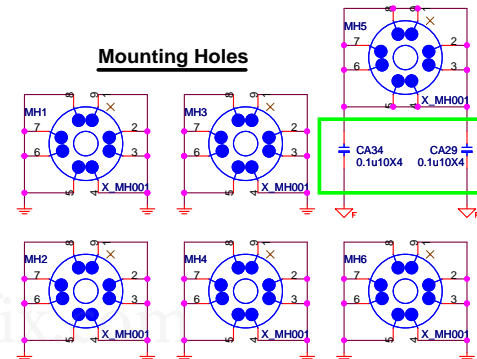
2015.08.10  
PCH H110 colay



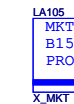
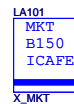
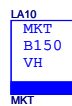
20150423 PM Request cost down



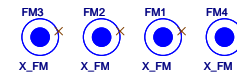
### Mounting Holes



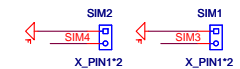
### Marketing Name貼紙



### Optical Fiducial Marks-120



### Simulation



7996\_13

2015/10/28 PK0-0799613-E48, 競華, 15, 寶安恩斯邁廠 (MSIS)  
2015/10/28 PK0-0799613-G37, 精成-深圳, 15, 寶安恩斯邁廠 (MSIS)